SENGUNTHAR ENGINEERING COLLEGE
(AUTONOMOUS)
(Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai)
Recognized Under Section 2(f) & 12(B) of the UGC Act, 1956
NAAC Accredited with 'A' Grade
TIRUCHENGODE - 637 205 NAMAKKAL (Dt) TAMILNADU

CURRICULUM & SYLLABI

M.E. VLSI DESIGN

(CHOICE BASED CREDIT SYSTEM)

REGULATIONS – 2023

(For the Students Admitted in the Academic Year 2023-2024 onwards)

Note: The regulations hereunder are subject to amendments as may be decided by the Academic Council of the Sengunthar Engineering College from time to time. Any or all such amendments will be effective from such date and to such batches of candidates including those already undergoing the program under the same Regulation as may be decided by the Academic Council.

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DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

REGULATION 2023

CURRICULUM AND SYLLABI

FOR M.E. – VLSI DESIGN

(For the Students admitted in the Academic Year 2023-2024 onwards)

FIRST SEMESTER

TO

FOURTH SEMESTER

INDEX

SCHEME FOR CURRICULUM

M.E. – VLSI Design

REGULATIONS 2023

CHOICE BASED CREDIT SYSTEM
M.E. VLSI DESIGN

VISION

- To be recognized as a premier centre in the field of Electronics and Communication Engineering by imparting professional, technical skills and research attitude to meet the developing needs of industry and society.

MISSION

- To impart technical education through effective teaching learning process in Electronics and Communication Engineering.
- To create research ambience to face the emerging technical challenges for the benefit of the society.
- To train the students to develop skills to solve complex technological problems and to make them competitive professionals through dynamic curriculum.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

Graduates can:

- ✓ Gain strong foundation in designing, testing, of electronic circuits relevant to the industry and society.
- ✓ Able to solve problems of social relevance and to provide innovative solutions through research with latest hardware and software related to VLSI.
- ✓ Develop attitude in lifelong learning, applying and adapting new ideas and technologies in VLSI domain.

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

PO1	**Engineering Knowledge**	Apply the basic knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems in Electronics and Communication Engineering field.
PO2	**Problem Analysis**	Identify, formulate, and analyze complex engineering problems reaching substantiated conclusions using mathematical principles and engineering sciences.
PO3	**Design / Development of Solutions**	Design system components or processes that meet the specified needs with appropriate consideration for the public health, cultural, societal, and environmental considerations.

PO4	**Conduct Investigations of Complex Problems**	Apply research-based knowledge and research methods including design of experiments, analysis and interpretation of data, pertaining to Electronics and Communication Engineering problems and arrive valid conclusions.
PO5	**Modern Tool Usage**	Create, select, and apply appropriate techniques, resources, and modern engineering tools required for Electronics and Communication Engineering applications.
PO6	**Engineer and Society**	Apply the contextual knowledge to assess societal, health, safety, and cultural issues and endure the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and Sustainability**	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics**	Apply ethical principles and commit to professional ethics and responsibilities and norms in the field of Electronics and Communication engineering.
PO9	**Individual and Teamwork**	Perform effectively as an individual, and as a member or leader in multidisciplinary teams.
PO10	**Communication**	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project Management and Finance**	Demonstrate knowledge and understanding of the engineering and management principles to manage projects and in multidisciplinary environment.
PO12	**Life-Long Learning**	Demonstrate resourcefulness for contemporary issues and lifelong learning.

PROGRAM SPECIFIC OUTCOME (PSOs)

PSO1	Specify, design and develop VLSI circuits to optimize power and area requirements, free from faults by modeling, simulation and testing.
PSO2	Design, develop and analyze VLSI systems by learning advanced algorithms, architectures and software-hardware co-design.
PSO3	Select, Architect and implement appropriate technologies to provide innovative solutions related to VLSI domain.

MAPPING OF COURSE OUTCOME AND PROGRAM OUTCOME

Year	Sem	Course Name	PO												PSO		
			1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
I	I	23PVM101- Graph Theory and Optimization Techniques	2.0	-	1.0	1.0	-	-	-	-	-	-	1.0	-	2.0	2.0	2.0
		23PGT101- Research Methodology and IPR	2.0	2.0	-	-	2.0	-	-	-	-	-	-	-	2.2	2.0	1.8
		23PVT101- Device Modeling	1.0	2.0	1.0	1.0	2.0	1.0	-	-	-	-	1.0	1.0	2.0	2.0	1.0
		23PVT102- System Design Using FPGA	1.0	1.0	1.0	1.0	1.0	-	-	-	-	-	1.0	1.0	2.0	2.0	1.0
		23PVE101- CMOS Digital VLSI Design	1.0	-	1.4	1.0	-	-	-	-	-	-	1.0	1.0	2.0	2.0	1.0
		Professional Elective - I	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		23PEE101- Research Paper Writing and Seminar	1.0	1.0	1.0	1.0	1.0	1.0	-	-	-	-	1.0	1.0	2.0	2.0	1.0
	II	23PVT201- Testing of VLSI Circuits	1.4	-	2.0	2.4	2.4	1.0	-	-	-	-	1.0	2.0	2.2	2.0	1.0
		23PVT202- CAD for VLSI Circuits	1.0	-	1.0	2.0	2.0	1.0	-	-	-	-	1.0	2.0	2.2	2.4	1.0
		23PVE201- Analog IC Design	1.0	1.0	2.0	1.0	1.0	-	-	-	-	-	1.0	2.0	2.4	2.6	1.0
		Professional Elective - II	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		Professional Elective - III	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		Open Elective - I	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		23PEE201- Mini Project	3.0	3.0	2.0	2.0	1.0	1.0	-	-	-	-	-	1.0	3.0	2.0	2.0
II	III	Professional Elective - IV	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		Professional Elective - V	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		Professional Elective - VI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		23PEE301- Project Work Phase - I	3.0	3.0	2.0	2.0	1.0	1.0	-	-	-	1.0	1.0	1.0	3.0	2.0	2.0
	IV	23PEE401- Project Work Phase - II	3.0	3.0	2.0	2.0	1.0	1.0	-	-	-	1.0	1.0	1.0	3.0	2.0	2.0

PROFESSIONAL ELECTIVE COURSES

S.No.	Course Name	PO												PSO		
		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
1	23PVP101- Low Power VLSI Design	2.0	-	2.0	2.0	2.0	-	-	-	-	-	2.0	2.0	2.0	2.0	1.0
2	23PVP102- DSP Integrated Circuits	1.0	-	1.0	1.0	-	-	-	-	-	-	1.0	2.0	1.0	2.0	1.0
3	23PVP103- Physical Design of VLSI Circuits	1.0	2.0	1.0	1.0	-	-	-	-	-	-	1.0	2.0	1.0	2.0	1.0
4	23PVP104- Advanced Computer Architecture and parallel Processing	1.0	2.0	2.0	1.0	1.0	-	-	-	-	-	1.0	2.0	1.0	2.0	1.0
5	23PVP105- VLSI Technology	1.0	-	2.0	2.0	1.0	-	-	-	-	-	1.0	1.0	2.0	2.0	1.0
6	23PVP201- VLSI Signal Processing	1.0	-	2.0	2.0	1	2.0	-	-	-	-	1.0	1.0	2.0	2.0	1.0
7	23PVP202- Reconfigurable Architectures	1.0	2.0	2.0	1.3	1.4	2.1	-	-	-	-	1.0	2.0	1.0	2.0	1.0
8	23PVP203- Design of Analog Filters and Signal Conditioning Circuits	1.2	2.6	2.0	1.2	1.0	-	-	-	-	-	1.0	3.0	1.0	2.0	1.0
9	23PVP204- System on Chip Design	1.2	1.2	2.0	1.2	1.1	-	-	-	-	-	1.0	2.4	1.4	2.0	1.0
10	23PVP205- Security Solutions in VLSI	1.2	3.0	2.6	1.2	2.0	-	-	-	-	-	1.0	2.8	1.2	2.6	1.0
11	23PVP206- Design of Semiconductor Memories	1.2	3.0	2.8	1.2	1.6	1.4	-	-	-	-	1.0	2.8	1.4	2.6	1.0
12	23PVP207- Scripting Languages for VLSI	1.2	2.0	2.6	1.2	1.4	1.4	-	-	-	-	1.0	2.8	1.4	2.6	1.0
13	23PVP208- Networks on Chip	1.0	-	1.0	2.2	-	-	-	-	-	-	1.0	2.4	1.6	2.6	1.0
14	23PVP209- Signal Integrity for High Speed Design	1.0	1.0	2.0	2.2	1.0	-	-	-	-	-	1.0	2.6	1.8	2.6	1.4
15	23PVP210- DSP Processor Architecture and Programming	1.0	2.0	1.0	1.0	2.0	-	-	-	-	-	1.0	2.0	1.4	2.2	1.4
16	23PVP301- Mixed Signal VLSI Design	1.0	2.0	1.0	1.0	2.0	2.0	-	-	-	-	1.0	2.0	1.0	2.2	1.4
17	23PVP302- Embedded System Design	1.0	1.0	2.0	2.0	3.0	1.0	-	-	-	-	1.0	3.0	1.0	2.0	1.2
18	23PVP303- Soft Computing and Optimization Techniques	1.0	-	2.0	1.0	2.0	-	-	-	-	-	1.0	2.0	1.4	2.0	1.0
19	23PVP304- VLSI for Biomedical Systems	1.0	1.6	1.0	1.0	1.0	-	-	-	-	-	1.0	-	1.0	2.0	1.0

20	23PVP305- RF IC Design	1.6	1.6	2.0	2.2	2.0	-	-	-	-	-	1.0	2.0	1.0	2.0	1.0
21	23PVP306- Hardware Verification Techniques	1.0	-	2.0	2.0	2.0	-	-	-	-	-	1.4	2.4	1.0	2.0	1.4
22	23PVP307- VLSI for Wireless Communication	1.0	2.0	3.0	2.0	1.2	1.0	-	-	-	-	1.0	-	1.0	2.0	1.0
23	23PVP308- ASIC Design	1.0	1.0	1.0	2.0	3.0	1.0	-	-	-	-	1.0	2.0	1.0	2.0	1.6
24	23PVP309- Nano Scale Devices	1.0	2.0	1.0	1.0	-	-	-	-	-	-	1.6	1.4	1.0	2.0	1.6
25	23PVP310- IP based VLSI Design	1.0	1.0	1.0	3.0	1.6	1.0	-	-	-	-	1.0	1.4	1.8	2.6	1.6
26	23PVP311- VLSI for IoT Systems	3.0	2.4	2.4	2.2	1.6	1.2	-	-	-	-	1.6	1.8	3.0	2.6	2.6
27	23PVP312- VLSI Architecture for Image and Video Processing	1.0	1.6	1.0	1.0	1.0	-	-	-	-	-	1.6	-	3.0	2.0	2.0
28	23PVP313- Hardware Software Co-Design	1.0	1.0	2.0	2.0	2.0	1.0	-	-	-	-	1.8	1.4	1.9	2.0	2.6
29	23PVP314- Selected Topics in IC Design	1.0	2.0	1.0	2.0	1.4	1.6	-	-	-	-	1.8	1.0	1.8	2.0	2.6
30	23PVP315- MEMS And NEMS	1.0	1.2	2.0	1.0	2.0	-	-	-	-	-	1.8	1.6	3.0	2.0	3.0

OPEN ELECTIVE COURSES

S.No.	Course Name	PO												PSO		
		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
31	23PGO201- Disaster Management	3.0	2.0	2.0	2.0	1.0	1.0	1.0	-	-	1.0	1.0	1.0	3.0	2.0	1.0
32	23PGO202 - Cost Management Of Engineering Projects	3.0	3.0	3.0	3.0	2.0	1.0	1.0	1.0	1.0	1.0	3.0	1.0	2.0	2.0	1.0
33	23PGO203 - Constitution Of India	3.0	2.0	2.0	1.0	-	1.0	-	1.0	1.0	1.0	-	1.0	2.0	1.0	1.0
34	23PGO204 - Business Analytics	3.0	3.0	3.0	3.0	2.0	1.0	-	1.0	1.0	1.0	2.0	1.0	3.0	2.0	1.0
35	23PGO205- Digital Marketing	3.0	3.0	3.0	3.0	2.0	1.0	-	1.0	1.0	1.0	1.0	1.0	3.0	2.0	1.0
36	23PGO206- Electronics In Solar Power	1.0	1.2	1.6	1.0	1.8	-	-	-	-	-	2.0	1.4	3.0	2.0	3.0

CURRICULUM AND SYLLABI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FOR M.E. VLSI DESIGN

(For the Students Admitted in the Academic Year 2023-2024 onwards)

FIRST SEMESTER

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
THEORY									
23PVM101	Graph Theory and Optimization Techniques	FC	3	1	0	4	40	60	100
23PGT101	Research Methodology and IPR	FC	3	0	0	3	40	60	100
23PVT101	Device Modeling	PC	3	0	0	3	40	60	100
23PVT102	System Design Using FPGA	PC	3	0	2	4	40	60	100
	Professional Elective - I	PE	3	0	0	3	40	60	100
EMBEDDED COURSE									
23PVE101	CMOS Digital VLSI Design	PC	3	0	2	4	40	60	100
EMPLOYABILITY ENHANCEMENT COURSE									
23PEE101	Research Paper Writing and Seminar	EEC	1	0	0	0	100	-	100
TOTAL CREDITS IN SEMESTER - I			21						

FC : Foundation Courses,
PC : Professional Core,
PE : Professional Elective,
OE : Open Elective,
EEC : Employability Enhancement Courses,
L : Lecture,
T : Tutorial,
P : Practical,
C : Credit Point,

CIA : Continuous Internal Assessment,
ESE : End Semester Examination,
TOT : Total

SECOND SEMESTER

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
THEORY									
23PVT201	Testing of VLSI Circuits	PC	3	0	0	3	40	60	100
23PVT202	CAD for VLSI Circuits	PC	3	0	0	3	40	60	100
	Professional Elective - II	PE	3	0	0	3	40	60	100
	Professional Elective - III	PE	3	0	0	3	40	60	100
	Open Elective - I	OE	3	0	0	3	40	60	100
EMBEDDED COURSE									
23PVE201	Analog IC Design	PC	3	0	2	4	40	60	100
EMPLOYABILITY ENHANCEMENT COURSE									
23PEE201	Mini Project	EEC	0	0	2	1	100	-	100
TOTAL CREDITS IN SEMESTER - II			20						

FC : Foundation Courses,
PC : Professional Core,
PE : Professional Elective,
OE : Open Elective,
EEC : Employability Enhancement Courses,
L : Lecture,
T : Tutorial,
P : Practical,
C : Credit Point,
CIA : Continuous Internal Assessment,
ESE : End Semester Examination,
TOT : Total

THIRD SEMESTER

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
THEORY									
	Professional Elective - IV	PE	3	1	0	4	40	60	100
	Professional Elective - V	PE	3	1	0	4	40	60	100
	Professional Elective - VI	PE	3	0	0	3	40	60	100
EMPLOYABILITY ENHANCEMENT COURSE									
23PEE301	Project Work Phase - I	EEC	0	0	12	6	40	60	100
TOTAL CREDITS IN SEMESTER - III			17						

FC : Foundation Courses,
PC : Professional Core,
PE : Professional Elective,
OE : Open Elective,
EEC : Employability Enhancement Courses,
L : Lecture,
T : Tutorial,
P : Practical,
C : Credit Point,
CIA : Continuous Internal Assessment,
ESE : End Semester Examination,
TOT : Total

FOURTH SEMESTER

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
EMPLOYABILITY ENHANCEMENT COURSE									
23PEE401	Project Work Phase - II	EEC	0	0	24	12	40	60	100
TOTAL CREDITS IN SEMESTER - IV			12						

FC : Foundation Courses,
PC : Professional Core,
PE : Professional Elective,
OE : Open Elective,
EEC : Employability Enhancement Courses,
L : Lecture,
T : Tutorial,
P : Practical,
C : Credit Point,
CIA : Continuous Internal Assessment,
ESE : End Semester Examination,
TOT : Total

LIST OF FOUNDATION COURSE (FC)

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PVM101	Graph Theory and Optimization Techniques	FC	4	0	0	4	40	60	100
23PGT101	Research Methodology and IPR	FC	3	0	0	3	40	60	100

LIST OF PROFESSIONAL CORE (PC)

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PVT101	Device Modeling	PC	3	0	0	3	40	60	100
23PVT102	System Design Using FPGA	PC	3	0	1	4	40	60	100
23PVE101	CMOS Digital VLSI Design	PC	3	0	2	4	40	60	100
23PVT201	Testing of VLSI Circuits	PC	3	0	0	3	40	60	100
23PVT202	CAD for VLSI Circuits	PC	3	0	0	3	40	60	100
23PVE201	Analog IC Design	PC	3	0	2	4	40	60	100

LIST OF PROFESSIONAL ELECTIVES COURSES

PROFESSIONAL ELECTIVE - I – SEMESTER I

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PVP101	Low Power VLSI Design	PE	3	0	0	3	40	60	100
23PVP102	DSP Integrated Circuits	PE	3	0	0	3	40	60	100
23PVP103	Physical Design of VLSI Circuits	PE	3	0	0	3	40	60	100
23PVP104	Advanced Computer Architecture and parallel Processing	PE	3	0	0	3	40	60	100
23PVP105	VLSI Technology	PE	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE- II – SEMESTER II

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PVP201	VLSI Signal Processing	PE	3	0	0	3	40	60	100
23PVP202	Reconfigurable Architectures	PE	3	0	0	3	40	60	100
23PVP203	Design of Analog Filters and Signal Conditioning Circuits	PE	3	0	0	3	40	60	100
23PVP204	System on Chip Design	PE	3	0	0	3	40	60	100
23PVP205	Security Solutions in VLSI	PE	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE- III – SEMESTER II

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PVP206	Design of Semiconductor Memories	PE	3	0	0	3	40	60	100
23PVP207	Scripting Languages for VLSI	PE	3	0	0	3	40	60	100
23PVP208	Networks on Chip	PE	3	0	0	3	40	60	100
23PVP209	Signal Integrity for High Speed Design	PE	3	0	0	3	40	60	100
23PVP210	DSP Processor Architecture and Programming	PE	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE-IV – SEMESTER III

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PVP301	Mixed Signal VLSI Design	PE	3	1	0	4	40	60	100
23PVP302	Embedded System Design	PE	3	1	0	4	40	60	100
23PVP303	Soft Computing and Optimization Techniques	PE	3	1	0	4	40	60	100
23PVP304	VLSI for Biomedical Systems	PE	3	1	0	4	40	60	100
23PVP305	RF IC Design	PE	3	1	0	4	40	60	100

PROFESSIONAL ELECTIVE-V – SEMESTER III

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PVP306	Hardware Verification Techniques	PE	3	1	0	4	40	60	100
23PVP307	VLSI for Wireless Communication	PE	3	1	0	4	40	60	100
23PVP308	ASIC Design	PE	3	1	0	4	40	60	100
23PVP309	Nano Scale Devices	PE	3	1	0	4	40	60	100
23PVP310	IP based VLSI Design	PE	3	1	0	4	40	60	100

PROFESSIONAL ELECTIVE-VI – SEMESTER III

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PVP311	VLSI for IoT Systems	PE	3	0	0	3	40	60	100
23PVP312	VLSI Architecture for Image and Video Processing	PE	3	0	0	3	40	60	100
23PVP313	Hardware – Software Co-Design	PE	3	0	0	3	40	60	100
23PVP314	Selected Topics in IC Design	PE	3	0	0	3	40	60	100
23PVP315	MEMS and NEMS	PE	3	0	0	3	40	60	100

LIST OF OPEN ELECTIVES

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PGO201	Disaster Management	OE	3	0	0	3	40	60	100
23PGO202	Cost Management of Engineering Projects	OE	3	0	0	3	40	60	100
23PGO203	Constitution of India	OE	3	0	0	3	40	60	100
23PGO204	Business Analytics	OE	3	0	0	3	40	60	100
23PGO205	Digital Marketing	OE	3	0	0	3	40	60	100
23PGO206	Electronics for Solar Power	OE	3	0	0	3	40	60	100

LIST OF EMPLOYABILITY ENHANCEMENT COURSES

Course Code	Name of the Subject	Category	Periods / Week			Credit	Maximum Marks		
			L	T	P	C	CIA	ESE	TOT
23PEE101	Research Paper Writing and Seminar	EEC	1	0	0	0	100	–	100
23PEE201	Mini Project	EEC	0	0	2	1	100	–	100
23PEE301	Project work (Phase – I)	EEC	0	0	12	6	40	60	100
23PEE401	Project work (Phase – II)	EEC	0	0	24	12	40	60	100

CURRICULUM AND SYLLABI

FOR M.E. DEGREE PROGRAMMES

(For the Students Admitted in the Academic Year 2023 – 2024 onwards)

CREDIT SUMMARY

M.E. – VLSI DESIGN

Category	Credits Per Semester				Credit Total
	I	II	III	IV	
FC	7	-	-	-	7
PC	11	10	-	-	21
PE	3	6	11	-	20
OE	-	3	-	-	03
EEC	0	1	6	12	19
Total	21	20	17	12	70

SCHEME FOR SYLLABI

M.E. – VLSI Design

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
FOR M.E. VLSI DESIGN

SEMESTER I

23PVM101 GRAPH THEORY AND OPTIMIZATION TECHNIQUES L T P C
3 1 0 4

OBJECTIVES

- To study the modern applications of graph theory using matrices and to study proof techniques related to various concepts in Trees.
- To learn proof techniques related to various concepts in Spanning Trees, Connectivity and planar graphs.
- To understand techniques of proofs in coloring and digraphs.
- To acquire the concepts of various linear programming methods.
- To know the concepts of duality, transportation model and assignment model.

UNIT I GRAPH THEORY **9+3**

Fundamental concepts of graph - Special types of Graphs - Walks, Paths and Circuits in graphs - Euler graphs - Hamiltonian graphs - Matrix representation of Graphs - Trees - Properties of Trees - Distance and Centers in a Tree - Rooted and binary Trees.

UNIT II CONNECTIVITY AND PLANARITY **9+3**

Spanning Trees - Spanning Trees in a weighted graph - Minimal spanning Trees - The algorithms of Kruskal and Prim - Cut-sets - Properties of a cut-set - Fundamental circuits and cut-sets - Connectivity and Separability - Planar graphs - Representations of a Planar graphs

UNIT III COLORING AND DIRECTED GRAPHS **9+3**

Chromatic number - Chromatic partitioning - Chromatic polynomial - Matchings - Coverings - The Four color problem - Digraphs - Types of Digraphs - Digraphs and binary relations - Euler Digraph.

UNIT IV LINEAR PROGRAMMING **9+3**

Introduction - Formulation of Linear Programming - Graphical method - Simplex method - Big M method – Two-phase method.

UNIT V DUALITY AND TRANSPORTATION MODEL **9+3**

Formulation of Dual problem - Application of Duality - Dual Simplex method - Definition of the Transportation Model - Nontraditional Transportation Models - The Transportation Algorithm - Assignment Model.

TOTAL: 45+15 = 60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Explain the basic concepts of graphs, different types of graphs and properties of Trees.
- Analyze the properties, theorems and be able to prove theorems.
- Apply suitable graph model and algorithm for solving applications.
- Discuss the optimization problems using Linear Programming methods.
- Examine integer programming and linear programming to solve real-life applications.

TEXT BOOKS

1. Narsingh Deo, "Graph Theory: With Applications to Engineering and Computer Science", Prentice Hall of India Learning Private Limited, Delhi, 2016.
2. Hamdy A. Taha, "Operations Research", Pearson Education, New Delhi, 2017.

REFERENCES

1. John Clark and Derek Allan Holton, "A First Look at Graph Theory", World ScientificPublishing Company, 2018.
2. Panneerselvam R, "Operations Research", PHI Learning private limited, 2019.

E-RESOURCES

1. https://nptel.ac.in/courses/111/106/111106102/(Graph Theory)
2. https://nptel.ac.in/courses/111/102/111102012/(Linear Programming Problems)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	2	-	1	1	-	-	-	-	-	-	1	-	2	2	2
2	2	-	1	1	-	-	-	-	-	-	1	-	2	2	2
3	2	-	1	1	-	-	-	-	-	-	1	-	2	2	2
4	2	-	1	1	-	-	-	-	-	-	1	-	2	2	2
5	2	-	1	1	-	-	-	-	-	-	1	-	2	2	2
AVG	2.0	-	1.0	1.0	-	-	-	-	-	-	1.0	-	2.0	2.0	2.0

1-Low 2-Medium 3-High '-' – No Correlation

23PGT101	RESEARCH METHODOLOGY AND IPR	L T P C
	(Common to all PG Engineering Courses)	3 0 0 3

OBJECTIVES

- To learn the problem formulation, analysis and solutions.
- To know the effective literature study approaches.
- To study Technical papers / presentations without violating professional ethics.
- To understand the process of process and procedure of patenting.
- To gain basic knowledge on intellectual property rights.

UNIT I RESEARCH PROBLEM **9**

Meaning of research problem – Sources of research problem – Criteria characteristics of a good research problem – Errors in selecting a research problem – Scope and objectives of research problem – Approaches of investigation of solutions for research problem – Data collection – Analysis – Interpretation – Necessary instrumentations

UNIT II LITERATURE REVIEW **9**

Effective literature studies approaches – Analysis – Plagiarism and research ethics.

UNIT III TECHNICAL WRITING /PRESENTATION **9**

Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR) **9**

Nature of Intellectual Property – Patents, Designs – Trade and Copyright – Process of Patenting and Development: technological research – Innovation, patenting, development – International Scenario: International cooperation on Intellectual Property – Procedure for grants of patents, Patenting under PCT.

UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR) **9**

Patent Rights: Scope of Patent Rights – Licensing and transfer of technology – Patent information and databases – Geographical Indications – New Developments in IPR: Administration of Patent System – IPR of Biological Systems, Computer Software etc – Traditional knowledge Case Studies, IPR and IITs.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the research problems.
- Apply effective literature studies in research work.
- Explain the effective technical papers/presentations.
- Discuss that today's world is controlled by Computer, Information Technology, but tomorrow the world will be ruled by ideas, concepts, and creativity.
- Explain the IPR and filing patents in R & D.

TEXT BOOKS

1. Ranjith Kumar, "Research Methodology: A step–by–step guide for beginners", SAGE Publications, Fourth Edition, 2017.
2. Neeraj Pandey, Khushdeep Dhrani, "Intellectual Property Rights", PHI Learning Private Limited, 2016.

REFERENCES

1. Heather Silyn–Roberts, "Writing for Science and Engineering: Papers, Presentations and Reports", Elsevier, second Edition, 2016.
2. Douglas C. Montgomery, "Design and Analysis of Experiments", Nineth Edition, Wiley Publishers, 2017.

E–RESOURCES

1. https://nptel.ac.in/courses/121/106/121106007/ (Introduction to Research)
2. https://nptel.ac.in/courses/109/106/109106137/ (IPR)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	2	2	2	2	1	-	-	-	-	**2**	1	2	1	2
2	3	2	2	2	2	1	-	-	-	-	2	1	2	1	2
3	3	2	1	1	1	1	-	-	-	-	2	1	2	1	1
4	3	2	2	2	2	1	-	-	-	-	2	1	2	1	1
5	3	2	1	1	1	1	-	-	-	-	2	1	2	1	1
AVG	**3.0**	**2.0**	**1.6**	**1.6**	**1.6**	**1.0**	**-**	**-**	**-**	**-**	**2.0**	**1.0**	**2.0**	**1.0**	**1.4**

1-Low 2-Medium 3-High '-' – No Correlation

23PVT101 **DEVICE MODELING** **L T P C**
3 0 0 3

OBJECTIVES

- To learn the basics of MOS physics and modeling of MOS structures.
- To gain knowledge in noise modeling and accurate distortion analysis in analogcircuits.
- To understand the concept of BSIM modeling and other MOSFET models
- To study the concept of non-quasi-static modeling and noise model temperature effects
- To acquire the knowledge of small signal modeling.

UNIT I BASIC DEVICE PHYSICS-I **9**

Two Terminal MOS Structure Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance; C-VCharacteristics.

Three Terminal MOS Structure

Contacting the inversion layer, Body effect, Regions of inversion, Pinch-off voltage.

UNIT II BASIC DEVICE PHYSICS-II **9**

Four Terminal MOS Transistor

Transistor regions of operation, general charge sheet models, regions of inversion in terms of terminal voltage, strong inversion, weak inversion, moderate inversion, interpolation models, effective mobility, temperature effects, breakdown p-channel MOS FET, enhancement and depletion type, model parameter values, model accuracy.

UNIT III MOS TRANSISTOR WITH ION-IMPLANTED CHANNELS **9**

Enhancement of nMOS, Depletion nMOS, Enhancement pMOS**.**

Small dimension effects: Channel length modulation, barrier lowering, two-dimensional charge sharing and threshold voltage, punch-through, carrier velocity saturation, hot carrier effects, scaling, effects of surface and drain series resistance, effects due to thin oxides and high doping. Sub threshold regions, short channel effects.

UNIT IV MOS TRANSISTOR IN DYNAMIC OPERATION **9**

Large Signal modeling: Quasi static operation, Terminal currents in Quasi static operation, Evaluation of Charges in Quasi static operation, Transit time under DC conditions, Limitations of Quasi static Model, Non Quasi static Analysis.

UNIT V SMALL SIGNAL MODELING FOR LOW, MEDIUM AND HIGH FREQUENCIES **9**

Low, Medium frequency small signal model for the intrinsic part, small signal model for Extrinsic Part, A complete Quasi static Model, Y-Parameter models, non-Quasi static Models.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss various characteristics of MOS Transistors..
- Analyze complex MOS device structures.
- Examine engineering problems with wide range of solutions in different MOSFET technologies.
- Design the characteristics of MOSFET in dynamic operation.
- Apply appropriate techniques, resources and tools to engineering activities in modelling MOS structures.

TEXT BOOKS

1. Yannis Tsividis, "Operation and modelling of the MOS Transistor", Oxford University press, 2018.
2. Trond Ytterdal,Yuhua cheng and Tor Fjeldly, "Device modelling for Analog and RF CMOS Circuit Design" Wiley publications,2017.

REFERENCES

1. Donald A Neamen and Dhrubes Biswas, "Semiconductor physics and Devices" Special Indian Edition,fourth edition,2015.
2. M.S.Tyagi, "Introduction to Semiconductor materials and Devices" Wiley, 2018.

E- RESOURCES

1. https://digimat.in/nptel/courses/video/117106033/L01 (Semiconductor modeling).
2. https://nptel.ac.in/courses/108/108/108108112/(Semiconductor Devices and Circuits)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	1	2	1	-	-	-	-	1	1	2	2	1
2	1	1	2	1	2	1	-	-	-	-	1	1	2	2	1
3	1	2	1	1	2	1	-	-	-	-	1	1	2	2	1
4	1	1	2	1	2	1	-	-	-	-	1	1	2	2	1
5	1	2	1	1	2	1	-	-	-	-	1	1	2	2	1
AVG	1.0	2.0	1.0	1.0	2.0	1.0	-	-	-	-	1.0	1.0	2.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVT102	SYSTEM DESIGN USING FPGA (Lab Embedded Course)	L T P C 3 0 2 4

OBJECTIVES

- To learn the advanced design and analysis of digital circuits with HDL.
- To acquire the depth knowledge of logic and system design.
- To gain knowledge for the design of advanced digital hardware systems with help of FPGA tools.
- To understand the concepts of FPGA and its architecture.
- To study about the System level Design.

UNIT I VERILOG HDL CODING STYLE **9**

Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - System Tasks & Compiler Directives - Test Bench - Data Flow Modeling - Behavioral level Modeling -Tasks & Functions.

UNIT II VERILOG MODELING OF COMBINATIONAL & SEQUENTIAL CIRCUITS **9**

Behavioral, Data Flow and Structural Realization – Adders – Multipliers- Comparators - Flip Flops Realization of Shift Register - Realization of a Counter- Synchronous and Asynchronous FIFO – Single port and Dual port RAM – Pseudo Random LFSR – Cyclic Redundancy Check.

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUIT **9**

State diagram-state table –state assignment-choice of flip-flops – Timing diagram –One hot encoding- Mealy and Moore state machines – Design of serial adder using Mealy and Moore state machines - State minimization – Sequence detection- Design of vending machine using One Hot Controller

UNIT IV FPGA AND ITS ARCHITECTURE **9**

Types of Programmable Logic Devices- PLA & PAL- FPGA Generic Architecture, ALTERA CycloneII Architecture – Timing Analysis and Power analysis using Quartus-II- SOPC Builder NIOS-II Soft- core Processor- System Design Examples using ALTERA FPGAs — Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, Keyboard, LCD.

UNIT V SYSTEM LEVEL DESIGN **9**

Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool(FPGA Advantage), Design flow using CPLDs and FPGAs. CASE STUDIES: Design considerations using CPLDs and FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

LIST OF EXPERIMENTS

1. Design and implementation of arithmetic circuits.
2. Design and implementation of real time clock and controller.
3. Design and implementation of memory modules and filters.
4. Interfacing with ADC/DAC and display modules.

TOTAL: 45+15= 60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the design and manually optimize complex combinational and sequential digital circuits.
- Design a model combinational and sequential digital circuits by Verilog HDL.
- Explain FPGA based systems, digital networks, architectures and large systems.
- Discuss various aspects in Large Scale Digital Systems design.
- Illustrate the process of interfacing and display modules.

TEXT BOOKS

1. S. Ramachandran, "Digital VLSI System Design: A Design Manual for implementation ofProjects on FPGAs and ASICs Using Verilog" Springer Publication, 2017.
2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis" Prentice Hall,Second Edition, 2015

REFERENCES

1. Mark Balch, "Complete Digital design – A Comprehensive Guide to Digital Electronics and Computer system Architecture," McGraw Hill, 2018.
2. Stephen Brown &Zvonko Vranesic, "Digital Logic Design with Verilog HDL" TATA McGrawHill Ltd. Second Edition, 2017.

E-RESOURCES

1. https://nptel.ac.in/courses/117/108/117108040/(Digital system design with PLDs and FPGAs)
2. http://www.nptelvideos.in/2012/12/digital-vlsi-system-design.html - (Digital VLSI System Design)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	1	1	1	-	-	-	-	-	1	1	2	2	1
2	1	1	1	1	1	-	-	-	-	-	1	1	2	2	1
3	1	1	1	1	1	-	-	-	-	-	1	1	2	2	1
4	1	1	1	1	1	-	-	-	-	-	1	1	2	2	1
5	1	1	1	1	1	-	-	-	-	-	1	1	2	2	1
6	1	1	1	1	1						1	1	2	2	1
AVG	1.0	1.0	1.0	1.0	1.0	-	-	-	-	-	1.0	1.0	2.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVE101 **CMOS DIGITAL VLSI DESIGN** **L T P C**
(Lab Embedded Course) **3 0 2 4**

OBJECTIVES

- To learn comprehensively with all aspects of transistor level design.
- To study the digital building blocks common to all CMOS microprocessors, DPSs, networkprocessors.
- To understand the basic concepts about MOS device and inverter characteristics II.
- To know the use of mathematical methods and circuit analysis models in analysis of CMOS digitalelectronics circuits, including logic components and their interconnect.
- To acquire the knowledge of static CMOS combinational and sequential logic at the transistor level, includingmask layout.
- To understand complete hardware level FGPA validation of important digital algorithms.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER **9**

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS **9**

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore"s constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS **9**

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier-based Registers, non bistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES **9**

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES **9**

Interconnect Parameters — Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

LIST OF EXPERIMENTS

1. Understanding Synthesis principles, Back annotation.
2. Test vector generation and timing analysis of sequential and combinational logic designrealized using HDL languages.
3. FPGA real time programming and I/O interfacing.
4. To plot the (i) output characteristics (ii) Transfer characteristics of an n-channel and p-channel MOSFET.
5. Design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.
6. Modeling and simulation of combinational and sequential circuits using verilog.

TOTAL: 45+15 = 60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Explain the mathematical methods and circuit analysis models in analysis of CMOS digital circuits.
- Analyze the models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logic effort.
- Discuss the sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches.
- Design a methodology of arithmetic building blocks.
- Apply the knowledge of CMOS in various clocking strategies processes.
- Illustrate the FGPA platform and carry out a serious of validation design.

TEXT BOOKS

1. Jan Rabaey, AnanthaChandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Prentice Hall of India, 2014.
2. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEEPress, Third Edition, 2018.

REFERENCES

1. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 2015.
2. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, Addision Wesley, 2014.

E-RESOURCES

1. https://onlinecourses.nptel.ac.in/noc21_ee09/(CMOS VLSI Design)
2. https://nptel.ac.in/courses/108/107/108107129/ (MOS Transistor)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	-	1	1	-	-	-	-	-	-	1	1	2	2	1
2	1	-	2	1	-	-	-	-	-	-	1	1	2	2	1
3	1	-	1	1	-	-	-	-	-	-	1	1	2	2	1
4	1	-	2	1	-	-	-	-	-	-	1	1	2	2	1
5	1	-	1	1	-	-	-	-	-	-	1	1	2	2	1
6	1	-	1	1	-	-	-	-	-		1	1	2	2	1
AVG	1.0	-	1.4	1.0	-	-	-	-	-	-	1.0	1.0	2.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PEE101 **RESEARCH PAPER WRITING AND SEMINAR** **L T P C**
1 0 0 0

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and thenplace it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (at least 15 journal papers).
4. Preparing a draft outline of research work.
5. Studying the papers and understanding the authors contributions and critically analyzing each paper.
6. Linking the papers and preparing a draft of the paper.
7. Preparing conclusions based on the reading of all the papers.
8. Writing the Final Paper and giving final Presentation.
9. Maintaining a file for records of activities.

Activities to be carried out

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic Stating an Objective	You are requested to select an area of interest, topic and state an objective	2nd week	**3 %**Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society. 2. List 2 journals 3. List 2 conferences, symposia or workshops. 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for papers (CFP) from your area.	3rd week	**3%**(the selected information must be area specific and of international and national standard)

Collection of Journal papers in the topic in the context of the objective —collect 20 &then filter	• You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read – try to: • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences, • Favour–firstIlor–foundational papers in the field (as indicated in other people's survey paper), • Favour more recent papers, • Pick a recent survey of the field so you can quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered	4th week	**6%**(the list of standard papers and reason for selection)
Reading and notes for first 5 papers	Reading Paper Process • For each paper form a Table answering the following questions • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)	5th week	**8%**(the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

Reading and notes for next5 papers	Repeat Reading Paper Process	6th week	**8%**(the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	**8%**(the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	**8%**(this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	**6%**(Clarity, purpose and conclusion) **6%** Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	**5%**(clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%**(this component will be evaluated based on the linking and classification amongthe papers)
Your conclusions	Write your conclusions and future work	12th week	**5%**(conclusions –clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th& 15th week	**10%**(based on presentation and Viva-voce)

TOTAL: 30 PERIODS

SEMESTER II

23PVT201 TESTING OF VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES

- To understand logic fault models.
- To learn test generation for sequential and combinational logic circuits.
- To acquire the concepts of testability.
- To know the self-test algorithms.
- To gain knowledge about fault diagnosis.

UNIT I VERILOG HDL CODING STYLE 9

Introduction to testing - Faults in Digital Circuits - Modeling of faults - Logical Fault Models - Faultdetection - Fault Location - Fault dominance – Logic simulation - Types of simulation - Delay models –Gate Level Event - driven simulation.

UNIT II TEST GENERATION 9

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability - Ad-hoc design - generic scan-based design - classical scan-based design - system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self-test - test pattern generation for BIST - Circular BIST - BIST Architectures - TestableMemory Design - Test Algorithms - Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze verilog HDL coding.
- Discuss test algorithms for Embedded RAMs.
- Design the testability.
- Explain test generation for combinational circuits.
- Analyze fault diagnosis for combinational circuits.

TEXT BOOKS

1. A.L.Crouch ,"Design Test for Digital IC's and embedded Core Systems ",Prentice Hall International, 2016.
2. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design",Jaico Publishing House, 2018.

REFERENCES

1. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory andMixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2019.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2015.

E-RESOURCES

1. https://onlinecourses.nptel.ac.in/noc20_ee76/preview(Digital VLSI Testing).
2. https://nptel.ac.in/courses/106/103/106103116/(Design Verification and Test of Digital VLSI circuits).

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	2	-	2	3	3	1	-	-	-	-	1	2	3	2	1
2	2	-	2	2	3	1	-	-	-	-	1	2	3	2	1
3	1	-	2	2	3	1	-	-	-	-	1	2	2	2	1
4	1	-	2	3	2	1	-	-	-	-	1	2	2	2	1
5	2	-	2	2	1	1	-	-	-	-	1	2	1	2	1
AVG	1.4	-	2.0	2..4	2.4	1.0	-	-	-	-	1.0	2.0	2.2	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVT202 **CAD FOR VLSI CIRCUITS** **L T P C**
3 0 0 3

OBJECTIVES

- To learn VLSI Design methodologies.
- To understand VLSI design automation tools.
- To design floor planning and routing.
- To study modeling and simulation.
- To gain knowledge of High level synthesis.

UNIT I INTRODUCTION TO VLSI DESIGN FLOW **9**

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II LAYOUT, PLACEMENT AND PARTITIONING **9**

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning.

UNIT III FLOOR PLANNING AND ROUTING **9**

Floor planning concepts, Shape functions and floor plan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV SIMULATION AND LOGIC SYNTHESIS **9**

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS **9**

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze VLSI design methodologies.
- Illustrate the layout, placement and partitioning.
- Explain floor planning and routing.
- Analyze Simulation and Logic Synthesis.
- Discuss the hardware models for high level synthesis.

TEXT BOOKS

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers,2017.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2020.

REFERENCES

1. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice",World Scientific 2016.
2. Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing, 2019.

E-RESOURCES

1. https://nptel.ac.in/courses/106/106/106106088/(CAD for VLSI Design).
2. https://onlinecourses.nptel.ac.in/noc21_cs96/preview(C-Based VLSI Design).

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	-	1	2	-	-	-	-	-	-	1	2	3	2	1
2	1	-	1	2	-	-	-	-	-	-	1	2	3	2	1
3	1	-	1	2	2	-	-	-	-	-	1	2	2	3	1
4	1	-	1	2	2	1	-	-	-	-	1	2	2	3	1
5	1	-	1	2	2	1	-	-	-	-	1	2	1	2	1
AVG	1.0	-	1.0	2.0	2.0	1.0	-	-	-	-	1.0	2.0	2.2	2.4	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVE201 **ANALOG IC DESIGN** **L T P C**
(Lab Embedded Course) **3 0 2 4**

OBJECTIVES

- To study MOS devices modelling and scaling effects.
- To learn the design of single stage and multistage MOS amplifier.
- To understand the analysis of single stage and multistage MOS amplifier frequency responses.
- To study the different design parameters in designing voltage reference circuit.
- To gain knowledge on OPAMP circuit.
- To know experiments to understand basic of VLSI based experiments.

UNIT I MOSFET METRICS **9**

Simple long channel MOSFET theory – SPICE Models – Technology trend, Need for Analog design - Sub-micron transistor theory, short channel effects, Narrow width effect, drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analog metrics, small signal parameters, Unity Gain Frequency, Miller's approximation.

UNIT II SINGLE STAGE AND TWO STAGE AMPLIFIERS **9**

Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers – differential and common mode response, Input swing, gain, diode load and constant current load - Basic Two Stage Amplifier, Cut-off frequency, poles and zeros.

UNIT III FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFERS **9**

Frequency Response of Single Stage Amplifiers - Noise in Single stage Amplifiers - Stability and Frequency Compensation in Single stage Amplifiers, Frequency Response of Two Stage Amplifiers-Noise in two stage Amplifiers – Stability, gain and phase margins, Frequency Compensation in two stage Amplifiers, Effect of loading in feedback networks.

UNIT IV CURRENT MIRRORS AND REFERENCE CIRCUITS **9**

Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design.

UNIT V OP AMPS **9**

Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, Noise, Output stage, OTA and OPAMP circuits – Low voltage OPAMP.

LIST OF EXPERIMENTS

1. Determination of small signal parameters.
2. Design and simulation of single stage amplifiers frequency response.
3. Design and simulation of differential amplifiers.
4. Design and simulation of operational amplifiers.
5. Design and simulation of data converters.
6. Design and simulation of PLL.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the performance characteristics of MOSFET Metrics.
- Examine single stage and Two stage Amplifiers.
- Analyze of single stage and multistage MOS amplifier frequency responses.
- Explain current mirrors and reference circuits.
- Illustrate MOS single stage, multistage amplifiers and OPAMP for desired frequencies.
- Discuss the simulated concepts of small signal parameters.

TEXT BOOKS

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2019.
2. Philip E.Allen, "CMOS Analog Circuit Design", Oxford University Press, 2013.

REFERENCES

1. Paul R.Gray, "Analysis and Design of Analog Integrated Circuits", Wiley Student edition, fifth edition, 2015.
2. R.Jacob Baker, "CMOS: Circuit Design, Layout , and Simulation", Wiley Student Edition, 2013.

E-RESOURCES

1. https://nptel.ac.in/courses/117/106/117106030/(Analog IC Design).
2. https://onlinecourses.nptel.ac.in/noc21_ee51/preview(Analog IC Design).

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	2	1	1	-	-	-	-	-	1	2	3	2	1
2	1	1	2	1	1	-	-	-	-	-	1	2	3	2	1
3	1	1	2	1	2	-	-	-	-	-	1	2	2	3	1
4	1	1	2	1	2	-	-	-	-	-	1	2	2	3	1
5	1	1	2	1	2	-	-	-	-	-	1	2	1	2	1
6	1	1	1	1	1	-	-	-	-	-	1	1	1	1	1
AVG	1.0	1.0	2.0	1.0	1.0	-	-	-	-	-	1.0	2.0	2.4	2.6	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PEE201 **MINI PROJECT** **L T P C**
0 0 2 1

OBJECTIVES

- To understand fabrication of one or more components working model, which is designed by them.
- To gain knowledge to fabricate any components using different manufacturing tools.

GUIDELINES

A student, under the supervision of a faculty member, shall collect literature on an allotted project topic of his / her choice, critically review the literature, carry out the mini project, and submit it to the department in a prescribed report form.

TOTAL: 30 PERIODS

EVALUATION PROCEDURE

The method of evaluation will be as follows:

1. Internal Marks (Continuous Assessment):100 marks.
   (Decided by review committee consist of HoD,Guide and senior faculty member conducting 3 reviews)

OUTCOMES

- At the end of the course project the students will understand the formulated industry / technical / societal problems. Analyze and / or develop models for providing solution to industry / technical / societal problems. Interpret and arrive at conclusions from the project carried out. Demonstrate effective communication skills through oral presentation. Engagein effective written communication through project report.

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	2	2	1	1	-	-	-	-	-	1	3	2	2
AVG	3.0	3.0	2.0	2.0	1.0	1.0	-	-	-	-	-	1.0	3.0	2.0	2.0

1-Low 2-Medium 3-High '-' – No Correlation

SEMESTER III

23PEE301	**PROJECT WORK PHASE–I**	**L T P C** **0 0 12 6**

OBJECTIVES

- To understand a specific problem for the current need of the society and collecting informationrelated to the same through detailed review of literature.
- To study the methodology to solve the identified problem.
- To train the students in preparing project reports and to face reviews and viva– voce examination.

GUIDELINES

The student individually works on a specific topic approved by faculty member who is familiar in this area of interest. The student can select any topic which is relevant to his/her specialization of the programme. The topic may be experimental or analytical or case studies. At the end of the semester, a detailed report on the work done should be submitted which contains clear definition ofthe identified problem, detailed literature review related to the area of work and methodology for carrying out the work. The students will be evaluated through a viva–voce examination by a panelof examiners including one external examiner.

TOTAL: 180 PERIODS

EVALUATION PROCEDURE

The method of evaluation will be as follows:

1. Internal Marks (Continuous Assessment):40 marks.
   (Decided by review committee consist of HoD, Guide and senior faculty member conducting 3 reviews)
2. End semester assessment (Evaluation of Project Report & Viva voce examination):60 marks. (Evaluated by the internal & external examiner appointed by the CoE and approval by HoD)

OUTCOMES

- At the end of the course project the students will have a clear idea of his/her area of work and they are in a position to carry out the remaining phase II work in a systematic way.

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	2	2	1	1	-	-	-	1	1	1	3	2	2
AVG	3.0	3.0	2.0	2.0	1.0	1.0	-	-	-	1.0	1.0	1.0	3.0	2.0	2.0

1-Low 2-Medium 3-High '-' – No Correlation

SEMESTER IV

23PEE401 **PROJECT WORK PHASE – II** **L T P C**
0 0 24 12

OBJECTIVES

- To understand the identified problem based on the formulated methodology.
- To learn skills to analyze and discuss the test results, and make conclusions.
- To train the students in preparing project reports and to face reviews and viva– voce examination.

GUIDELINES

The student should continue the phase–I work on the selected topic as per the formulated methodology. At the end of the semester, after completing the work to the satisfaction of the supervisor and review committee, a detailed report should be prepared and submitted to the head of the department. The students will be evaluated through based on the report and the viva-voce examination by a panel of examiners including one external examiner.

TOTAL: 360 PERIODS

EVALUATION PROCEDURE

The method of evaluation will be as follows:

1. Internal Marks (Continuous Assessment): 40 marks.
   (Decided by review committee consist of HoD, Guide and senior faculty member conducting 3 reviews)
2. End semester assessment (Evaluation of Project Report & Viva voce examination): 60 marks. (Evaluated by the internal & external examiner appointed by the CoE and approval by HoD)

OUTCOMES

- On completion of the project work students will be in a position to take up any challengingpractical problem and find better solutions.

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	2	2	1	1	-	-	-	1	1	1	3	2	2
AVG	3.0	3.0	2.0	2.0	1.0	1.0	-	-	-	1.0	1.0	1.0	3.0	2.0	2.0

1-Low 2-Medium 3-High '-' – No Correlation

PROFESSIONAL ELECTIVE I

23PVP101 LOW POWER VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES

- To learn sources of power in an IC.
- To understand power reduction techniques based on technology independent and technologydependent.
- To study the power dissipation mechanism in various MOS logic style.
- To learn suitable techniques to reduce the power estimation.
- To acquire sound knowledge about software design for low power.

UNIT I POWER DISSIPATION IN CMOS 9

Physics of power dissipation in CMOS FET devices - Hierarchy of limits of power - Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers andtheir performance comparison.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – low voltage low power static Randomaccess and dynamic Random-access memories – low power clock, Inter connect and layoutdesign – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION 9

Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the basics and advanced techniques in low power design.
- Examine low power VLSI optimized circuits.
- Discuss thesuitable techniques of low power CMOS circuits.
- Examine reduction in power estimation by an IC earns a lot including reduction in size, costand etc.
- Analyze synthesis and software design of low power.

TEXT BOOKS

1. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 2016.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer, 2014.

REFERENCES

1. Dimitrios Soudris, C.Pignet, Costas Goutis,"Designing CMOS Circuits for Low Power" Kluwer, 2012.
2. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 2019.

E- RESOURCES

1. https://nptel.ac.in/courses/106/105/106105034/ (Low power VLSI circuits and systems)
2. https://nptel.ac.in/courses/117/101/117101004 /- (Advanced VLSI Design)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	2	-	2	3	2	-	-	-	-	-	1	2	3	2	1
2	2	-	2	2	2	-	-	-	-	-	2	2	3	2	1
3	1	-	2	2	2	-	-	-	-	-	2	2	2	3	1
4	1	-	2	3	2	-	-	-	-	-	2	2	2	3	1
5	2	-	2	2	3	-	-	-	-	-	1	2	1	2	1
AVG	2.0	-	2.0	2.0	2.0	-	-	-	-	-	2.0	2.0	2.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP102 **DSP INTEGRATED CIRCUITS** **L T P C**
3 0 0 3

OBJECTIVES

- To learn the mapping of DSP system design onto hardware.
- To study the fundamental power management concepts of signal processing.
- To understand different DSP architectures and processing elements.
- To gain knowledge about uniprocessor in Digital Signal Processing.
- To acquire sound knowledge about Processing elements of IC.

UNIT I DSP SYSTEM DESIGN **9**

FFT Processor, Design Iteration Scheduling Loop-Folding - Cyclic Scheduling Formulation - Overflow and Quantization - Scheduling Algorithms - FFT Processor- Resource Allocation- Partitioning and Assignment Interpolator- Processor - Memory Assignment Butterfly Processor DCT Processor.

UNIT II DIGITAL SIGNAL PROCESSOR **9**

DSPs and microprocessors - embodiment, alternatives - memory architecture - addressing- pipelining – on - chip debugging, power consumption and management - clocking - application support - choosing processor architecture trends. Standard digital signal processors - Application specific IC's for DSP.

UNIT III DSP ARCHITECTURES **9**

Standard DSP and Ideal DSP architectures- Multiprocessors and multicomputer- message based architectures Systolic and Wave front arrays, Shared memory architectures. SHARC and Blackfin processors - Architecture overview, memory management - I/O management- On chip resources - programming considerations, Real time implementations.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES **9**

Mapping of DSP algorithms onto hardware - Uniprocessor architectures- Isomorphic mapping of SFGs, Implementation based on complex PEs- vector-multiplier based implementations- numerically equivalent implementation, implementation of WDFs, Shared memory architecture with Bit – serial PEs, building the large DSP systems- Single Instruction Computer (SIC).

UNIT V PROCESSING ELEMENTS OF IC **9**

Bit-Serial Arithmetic- Bit-Serial Two-Port Adaptor 8 S/P Multipliers With Fixed Coefficients Minimum Number Of Basic Operations- Bit-Serial Squares- Serial/Serial Multipliers- Digit-Serial Arithmetic, Cordic Algorithm - Distributed Arithmetic- The Basic Shift-Accumulator - Reducing The Memory Size -Complex Multipliers - Improved Shift Accumulator FFT Processor-Twiddle Factor PE- Control PEs, Address PEs, Base Index Generator, Ram Address PEs.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Illustrate the DSP System design.
- Discuss the design and methodologies in hardware and software design.
- Analyze the different architectures in Digital Signal Processor.
- Express the knowledge about synthesis of DSP architectures.
- Explain the different processing elements in DSP IC.

TEXT BOOKS

1. B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2014.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education, 2018.

REFERENCES

1. Keshab Parhi, "VLSI Digital Signal Processing Systems design & Implementation", John Wiley & Sons, 2015.
2. Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 2017.

E-RESOURCES

1. http://www.nptelvideos.in/2012/11/digital-integrated-circuits (DSP Integrated Circuits)
2. https://www.digimat.in/nptel/courses/video/108108111/L01 (Introduction to IC)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	-	1	1	-	-	-	-	-	-	1	2	1	2	1
2	1	-	1	1	-	-	-	-	-	-	1	2	1	2	1
3	1	-	1	1	-	-	-	-	-	-	1	2	1	2	1
4	1	-	1	1	-	-	-	-	-	-	1	2	1	2	1
5	1	-	1	1	-	-	-	-	-	-	1	2	1	2	1
AVG	1.0	-	1.0	1.0	-	-	-	-	-	-	1.0	2.0	1.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP103 PHYSICAL DESIGN OF VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES

- To acquire knowledge on fundamentals of VLSI technology.
- To study rules of layout, partitioning, floor planning,
- To understand placement and routing algorithms.
- To gain knowledge on various performance issues in circuit Layout.
- To know an exposure for cell generation and compaction.

UNIT I INTRODUCTION TO VLSI TECHNOLOGY 9

Layout Rules - Circuit abstraction Cell generation using programmable logic array transistor chaining - Wein Berger arrays and gate matrices - layout of standard cells gate arrays and sea of gates - Field Programmable Gate Array (FPGA) - layout methodologies Packaging - Computational Complexity - Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan - Lin Heuristic Ratio cut partition with capacity and I/O constraints. Floor planning: Rectangular dual floor planning hierarchical approach - simulated annealing - Floor plan sizing. Placement: Cost function - force directed method - placement by simulated annealing partitioning placement - module placement ona resistive network - regular placement linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running - line searching- Steiner trees Global Routing: Sequential Approaches - hierarchical approaches - multi commodity flow based techniques - Randomized Routing - One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA - Row based FPGAs.

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing - Driven Placement: Zero Stack Algorithm- Weight based placement - Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem - Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization.

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION 9

Planar subset problem (PSP) - Single Layer Global Routing - Single Layer detailed Routing - Wire length and bend minimization technique - Over The Cell (OTC) Routing Multiple chip modules (MCM) - programmable Logic Arrays - Transistor chaining - Wein Burger Arrays - Gate matrix layout - 1D compaction - 2D compaction.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Explain the layout rules and layout methodologies.
- Discuss the implementation of partitioning, floor planning, placement and routing of the cells.
- Analyze routing using top down approach.
- Examine the performance issues in circuit layout.
- Apply 1D and 2D compaction techniques.

TEXT BOOKS

1. Majid Sarrafzadeh, C. K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill, 2016.
2. Andrew B. Kahng, Jens Lienig, Igor L. Markov, JinHu , "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer Publications, 2018.

REFERENCES

1. Sung Kyu Lim, "Practical Problems in VLSI Physical Design Automation", Springer Publications, 2016.
2. Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 2017.

E - RESOURCES

1. https://nptel.ac.in/courses/106/105/106105161/ (VLSI Physical Design)
2. https://nptel.ac.in/courses/117/103/117103125/ (VLSI Design verification and test)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	1	-	-	-	-	-	-	1	2	1	2	1
2	1	2	1	1	-	-	-	-	-	-	1	2	1	2	1
3	1	2	1	1	-	-	-	-	-	-	1	2	1	2	1
4	1	2	1	1	-	-	-	-	-	-	1	2	1	2	1
5	1	2	1	1	-	-	-	-	-	-	1	2	1	2	1
AVG	1.0	2.0	1.0	1.0	-	-	-	-	-	-	1.0	2.0	1.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP104	ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	L T P C 3 0 0 3

OBJECTIVES

- To understand the difference between the pipeline and parallel concepts.
- To study the various types of architectures and the importance of scalable architectures.
- To know the various memories and optimization of memory.
- To learn the concepts of multiprocessors.
- To gain knowledge the concepts of Multi-core architectures.

UNIT I COMPUTER DESIGN AND PERFORMANCE MEASURES **9**

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors – Multi vector and SIMD architectures – Multithreaded architectures – Data-flow architectures – Performance Measures.

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP **9**

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Overcoming Data Hazards with Dynamic Scheduling - Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.

UNIT III MEMORY HIERARCHY DESIGN **9**

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.

UNIT IV MULTIPROCESSORS **9**

Symmetric and distributed shared memory architectures – Cache coherence issues - Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V MULTI-CORE ARCHITECTURES **9**

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case Studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss performance evaluation issues, data representation and fixed arithmetic.
- Examine the Concept of Parallel Processing and its applications.
- Analyze and evaluate the organization and functioning of hierarchical memory, cache organizational schemes, and virtual memory.
- Illustrate the introduction of memory architecture.
- Explain Software and Hardware multithreading.

TEXT BOOKS

1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2015.
2. John L. Hennessey and David A. Patterson, "Computer Architecture - A quantitative approach", Morgan Kaufmann / Elsevier, Fourth edition, 2017.

REFERENCES

1. William Stallings, "Computer Organization and Architecture – Designing for Performance", Pearson Education, Seventh Edition, 2016.
2. John P. Hayes, "Computer Architecture and Organization", McGraw Hill.

E - RESOURCES

1. https://nptel.ac.in/courses/106/103/106103206/ (Advanced computer architecture)
2. https://nptel.ac.in/courses/106/104/106104024/ (Parallel computer architecture)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	2	1	1	-	-	-	-	-	1	2	1	2	1
2	1	2	2	1	1	-	-	-	-	-	1	2	1	2	1
3	1	2	2	1	1	-	-	-	-	-	1	2	1	2	1
4	1	2	2	1	1	-	-	-	-	-	1	2	1	2	1
5	1	2	2	1	1	-	-	-	-	-	1	2	1	2	1
AVG	1.0	2.0	2.0	1.0	1.0	-	-	-	-	-	1.0	2.0	1.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP105 VLSI TECHNOLOGY L T P C
3 0 0 3

OBJECTIVES

- To study the different properties of material.
- To know various oxide formation techniques.
- To understand plasma assisted etching methods.
- To learn the various pattern generation techniques.
- To acquire the concept of circuit fabrication.

UNIT I MATERIAL PROPERTIES & CRYSTAL GROWTH 9

Crystal structure-axes &planes, Crystal defects-Point defects &dislocation crystal growth – Bridgman Czochralski techniques & Zone process, Doping in the melt. DIFFUSION & ION IMPLANTATION: Nature of diffusion – interstitial, Substitutional, interstitial Substitutional movements, Diffusion constant, Dissociate process, diffusion equation – D is constant & function, Diffusion systems, problems in Si diffusion, Evaluation techniques Ion implantation: Penetration range , implantation Damage, Annealing Implantation systems.

UNIT II OXIDATION AND EPITAXY OXIDATION 9

Themal oxidation –Intrinsic, Extrinsic Silicon Glass, Oxide formation ,Kinetic of oxide growth, Oxidation systems ,Faults Anodic oxidation, EPITAXY: Vapour Phase Epitaxy (VPE)- transport, reaction and growth ,Chemistry of growth, Institu etching, selective epitaxy, imperfections, Liquid Phase Epitaxy, LPE system ,Evaluation of epitaxial layers.

UNIT III ETCHING 9

ETCHING: Wet chemical etching, anisotropic etchants, Etching for non crystalline films, Plasma etching, Plasma assisted etching cleaning.

UNIT IV LITHOGRAPHY 9

Pattern generation and Masking, Printing and Engraving, Optical E-beam, ion beam X ray, Photo resists, defects.

UNIT V DEVICE AND CIRCUIT FABRICATION 9

ISOLATION Mesa, Oxide .PN junction isolation ,Self alignment, local oxidation, Planarisation, Metallization and packaging. Circuits – N,P and CMOS transistors, memory devices ,BJT circuits – buried layers ,PNP and NPN transistors, Diodes ,Resistors, Capacitors.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss the material properties and crystal growth.
- Explain the oxidation techniques.
- Analyze various etching techniques.
- Illustrate printing and engraving methods.
- Examine various device fabrication concepts.

TEXT BOOKS

1. Donald Neamen, Dhrupes Biswas , "Semiconductor Physics and Devices" McGraw Hill, New York , Fourth Edition, 2017.
2. Massimo Rudan, "Physics of Semiconductor devices"Springer ,Second Edition, 2017.

REFERENCES

1. Sze S M, "VLSI Technology "McGraw Hill ,New York ,Second Edition,2017.
2. Chang SY and Sze S M, "VLSI Technology"McGraw Hill ,New York ,2014.

E- RESOURCES

1. https://nptel.ac.in/courses/117/106/117106093/ (VLSI Technology)
2. https://nptel.ac.in/courses/108/101/108101089/ (Fabrication of VLSI Circuits using the MOS Technology)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	-	2	2	1	-	-	-	-	-	1	1	2	2	1
2	1	-	2	2	1	-	-	-	-	-	1	1	2	2	1
3	1	-	2	2	1	-	-	-	-	-	1	1	2	2	1
4	1	-	2	2	1	-	-	-	-	-	1	1	2	2	1
5	1	-	2	2	1	-	-	-	-	-	1	1	2	2	1
AVG	1.0	-	2.0	2.0	1.0	-	-	-	-	-	1.0	1.0	2.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlatio

PROFESSIONAL ELECTIVE II

23PVP201 VLSI SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES

- To learn techniques for altering the existing DSP structures to suit VLSI implementations.
- To understand the algorithmic reduction techniques.
- To know the fast convolution, IIR filters.
- To study an exposure for various Bit-level Arithmetic architectures.
- To gaint knowledge on various algorithmic strength reduction techniques.

UNIT I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE - I 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms - 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III ALGORITHIMIC STRENGTH REDUCTION - II 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon"s bit-serial multipliers using Horner"s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner"s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

UNIT V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING **9**

Numerical strength reduction - subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss the pipelining and parallel processing of digital filters.
- Analyze the concept of pipelining, retiming and parallel processing in design of high-speed low power applications.
- Apply unfolding, folding and fast convolution in the design of VLSI architecture
- Explain the bit-level arithmetic architectures..
- Employ the algorithmic strength reduction techniques to VLSI implementation of filters.

TEXT BOOKS

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", Wiley, Interscience, 2017.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2014.

REFERENCES

1. Doebelin, E.O., Measurement Systems - Application and Design, Tata McGraw Hill publishing company, 2015.
2. R.K Rajput, Electrical Measurements and Measuring Instruments, S.Chand & Company LTD, 2019.

E-RESOURCES

1. https://nptel.ac.in/courses/108/105/108105157/(VLSI Signal Processing)
2. https://onlinecourses.nptel.ac.in/noc20_ee44/preview(VLSI Signal Processing)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	-	2	2	1	2	-	-	-	-	1	1	2	2	1
2	1	-	2	2	1	2	-	-	-	-	1	1	2	2	1
3	1	-	2	2	1	2	-	-	-	-	1	1	2	2	1
4	1	-	2	2	1	2	-	-	-	-	1	1	2	2	1
5	1	-	2	2	1	2	-	-	-	-	1	1	2	2	1
AVG	1.0	-	2.0	2.0	1.0	2.0	-	-	-	-	1.0	1.0	2.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP202 **RECONFIGURABLE ARCHITECTURES** **L T P C**
3 0 0 3

OBJECTIVES

- To understand concept of reconfigurable computing systems.
- To acquire knowledge on fundamentals of reconfigurable architectures.
- To study flexibility on rout ability.
- To learn the FPGA based on the basic blocks, application specific design styles.
- To study the routing of FPGA, Technology independent optimization, high level synthesis and RCS for specific applications.

UNIT I INTRODUCTION **9**

Domain-specific processors, Application specific processors, Reconfigurable Computing Systems – Evolution of reconfigurable systems – Characteristics of RCS advantages and issues. Fundamental concepts & Design steps – classification of reconfigurable architecture-fine, coarse grain & hybrid architectures – Examples.

UNIT II FPGA TECHNOLOGIES & ARCHITECTURE **9**

Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.

UNIT III ROUTING FOR FPGAS **9**

General Strategy for routing in FPGAs- routing for row-based FPGAs – segmented channel routing, definitions - Algorithm for I segment and K segment routing – Routing for symmetrical FPGAs, Flexibility of FPGA Routing Architectures: FPGA architectural flexibility on Routability - Effect of switch block flexibility on routability - Tradeoffs in flexibility of S and C blocks.

UNIT IV HIGH LEVEL DESIGN **9**

FPGA Design style: Technology independent optimization- technology mapping- Placement. High level synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cycle based, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic) - verification physical design tools.

UNIT V APPLICATION DEVELOPMENT WITH FPGAS **9**

Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the reconfigurable architecture and FPGA fundamentals.
- Illustrate FPGA routing architectures.
- Examine the routing for FPGA .
- Explain high level synthesis.
- Discuss the applications development with FPGA.

TEXT BOOKS

1. Christophe Bobda, "Introduction to Reconfigurable Computing –Architectures, Algorithms and Applications", Springer, 2015.
2. Clive "Max" Maxfield, "The Design Warrior"s Guide to FPGAs: Devices, Tools And Flows", Newnes, Elsevier, 2016.

REFERENCES

1. Jorgen Staunstrup, Wayne Wlf, "Hardware/Software Co- Design: Principles and practice", Kluwer Academic Pub, 2017.
2. Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation, edited by Scott Hauck and Andre De Hon, Elsevier, Inc. (Morgan Kaufmann Publishers), Amsterdam, 2018.

E - RESOURCES

1. https://nptel.ac.in/courses/108/105/108105118/(Architectural Design of Digital Integrated Circuits)
2. https://nptel.ac.in/courses/117/108/117108040/(Digital System Design with PLDs and FPGAs)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	2	1	1	2	-	-	-	-	1	2	1	2	1
2	2	2	2	2	1	2	-	-	-	-	1	2	1	2	1
3	1	2	2	1	2	3	-	-	-	-	1	2	2	2	1
4	1	2	2	1	2	2	-	-	-	-	1	2	2	2	1
5	1	2	2	1	1	2	-	-	-	-	1	2	1	2	1
AVG	1.0	2.0	2.0	1.3	1.4	2.1	-	-	-	-	1.0	2.0	1.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP203	DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS	L T P C 3 0 0 3

OBJECTIVES

- To understand the concepts of filter topologies.
- To learn the functions of integrator.
- To study an exposure for switched capacitor filter realization.
- To know the discussion about signal conditioning techniques.
- To gain knowledge on signal conditioning circuits.

UNIT I FILTER TOPOLOGIES **9**

The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad.

UNIT II INTEGRATOR REALIZATION **9**

Lowpass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active RC SNR, gm-C Integrators, Discrete Time Integrators.

UNIT III SWITCHED CAPACITOR FILTER REALIZATION **9**

Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.

UNIT IV SIGNAL CONDITIONING TECHNIQUES **9**

Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.

UNIT V SIGNAL CONDITIONING CIRCUITS **9**

Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Transimpedance Amplifiers, Charge Amplifiers, Noise in Amplifiers.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the concepts filter topologies.
- Examine the integrator realization.
- Discuss the concept of switched capacitor filter realization.
- Apply the concepts of signal conditioning techniques.
- Explain the signal conditioning circuits.

TEXT BOOKS

1. Ramson Pallas-Areny, John G. Webster "Sensors and Signal Conditioning", A Wiley Interscience Publication, John Wiley & Sons INC, 2020.
2. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", John Wiley & Sons, 2018.

REFERENCES

1. Schauman, Xiao and Van Valkenburg, "Design of Analog Filters", OxUniversity Press,2019.
2. Hayes and Horowitz, Learning the Art of Electronics: A Hands-On Lab Course, 2016.

E-RESOURCES

1. https://nptel.ac.in/courses/117/108/117108107/(Analog Circuits and Systems)
2. https://nptel.ac.in/courses/108/105/108105064/(Industrial Instrumentation)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	2	1	1	-	-	-	-	-	1	3	1	2	1
2	2	2	2	2	1	-	-	-	-	-	1	3	1	2	1
3	1	3	2	1	1	-	-	-	-	-	1	3	2	2	1
4	1	3	2	1	1	-	-	-	-	-	1	3	2	2	1
5	1	3	2	1	1	-	-	-	-	-	1	2	1	2	1
AVG	1.2	2.6	2.0	1.2	1.0	-	-	-	-	-	1.0	3.0	1.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP204 **SYSTEM ON CHIP DESIGN** **L T P C**
3 0 0 3

OBJECTIVES

- To understand CMOS scaling, integration and system on chip.
- To Know the various operating principle of ASIC, CSIC, RISC applications.
- To study the discussion of NSIC, ADL Languages.
- To gain the knowledge SOC related modeling.
- To understand an exposure on Low power SOC and Digital system.

UNIT I MOTIVATION FOR SOC DESIGN **9**

Review of Moore's law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance, Comparison of System-on-Board, System-on-Chip, and System-in-Package, Typical goals in SOC design–cost reduction, power reduction, design effort reduction, performance maximization.

UNIT II ASIC **9**

Overview of ASIC types, Design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application specific Instruction Processor(ASIP)concepts.

UNIT III NISC **9**

No instruction set computer(NISC) Control words methodology, NISC Application and Advantages, Architecture Description Languages(ADL) for design and verification of Application specific Instruction set Processors(ASIP), No-Instruction-set computer (NISC) - design flow, modeling NISC architectures and systems, use of generic netlist representation.

UNIT IV SIMULATION **9**

Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SOC related modeling of data path design and control logic, Minimization of interconnect impact, clock tree issues.

UNIT V LOW POWER SOC DESIGN/DIGITAL SYSTEM **9**

Design synergy, Low power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling(DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Examine SoB, SoC and SiP for electronic product in terms of size, cost, performance and reliability.
- Analyze different approaches for solving architectural issues of SOC design.
- Discuss NISC and use of ADL.
- Explain different simulation models and modeling of reconfigurable systems.
- Illustrate low power SOC design.

TEXT BOOKS

1. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System onChip Interconnect", Morgan Kaufmann Publishers, 2018.
2. Rao R. Tummala, Madhavan Swaminathan, "Introduction to system on package SOP – Miniaturization of the Entire System", McGraw-Hill, 2017.

REFERENCES

1. Hubert Kaselin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2017.
2. Michael J Flynn and Wayne Luk, "Computer system design: System-on-chip", Wiley Publications, 2015.

E - RESOURCES

1. https://nptel.ac.in/courses/108106158 (Digital IC Design)
2. https://nptel.ac.in/courses/108/102/108102045/ (Embedded system)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	2	1	1	-	-	-	-	-	1	3	1	2	1
2	2	2	2	2	1	-	-	-	-	-	1	3	1	2	1
3	1	1	2	1	1	-	-	-	-	-	1	3	2	2	1
4	1	1	2	1	1	-	-	-	-	-	1	3	2	2	1
5	1	1	2	1	1	-	-	-	-	-	1	2	1	2	1
AVG	1.2	1.2	2.0	1.2	1.1	-	-	-	-	-	1.0	2.4	1.4	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP205 **SECURITY SOLUTIONS IN VLSI** **L T P C**
3 0 0 3

OBJECTIVES

- To study the different kinds of threats to information security.
- To learn the various techniques for data encryption.
- To know the case study based on VLSI for security threats.
- To acquire a design and implement the various cryptography algorithms in VLSI.
- To understand the concepts of crypto chip design.

UNIT I BASIC CONCEPTS **9**

Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS, Targets: Hardware, Software, Data communication procedures. Threats to Security: Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security.

UNIT II ENCRYPTION TECHNIQUES **9**

Conventional techniques, Modern techniques,DES, DES chaining+, Triple DES, RSA algorithm, Key management. Message Authentication and Hash Algorithm: Authentication requirements and functions secure Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service.

UNIT III FIREWALLS AND CYBER LAWS **9**

Firewalls, Design Principles, Trusted systems, IT act and cyber laws, Virtual private network.

UNIT IV FUTURE THREATS TO NETWORK **9**

Recent attacks on networks, VLSI Based Case study.

UNIT V CRYPTO CHIP DESIGN **9**

VLSI Implementation of AES algorithm, Implementation of DES, IDEA AES algorithm, Developmentof digital signature chip using RSA algorithm.

TOTAL : 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss the basic concepts of Information system.
- Analyze the data encryption techniques.
- Examine the firewalls and cyber laws.
- Illustrate the future threats to network.
- Analyze the concepts of crypto chip design.

TEXT BOOKS

1. William Stalling "Cryptography and Network Security" Pearson Education, 2015.
2. Charels P. Pfleeger "Security in Computing" Prentice Hall, 2016.

REFERENCES

1. Jeff Crume "Inside Internet Security" Addison Wesley, 2010.
2. Charlie Kaufman, "Network Security Private Communication in Public World" Second edition,Prentice Hall of India New Delhi, 2014.

E-RESOURCES

1. https://nptel.ac.in/courses/106/105/106105162/(Crptography and Network Security)
2. https://nptel.ac.in/courses/106/106/106106178/(Information security)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	3	2	1	2	-	-	-	-	-	1	3	1	2	1
2	2	3	3	2	2	-	-	-	-	-	1	3	1	3	1
3	1	3	3	1	2	-	-	-	-	-	1	3	2	3	1
4	1	3	3	1	2	-	-	-	-	-	1	3	2	3	1
5	1	3	2	1	2	-	-	-	-	-	1	2	1	2	1
AVG	1.2	3.0	2.6	1.2	2.0	-	-	-	-	-	1.0	2.8	1.2	2.6	1.0

1-Low 2-Medium 3-High '-' – No Correlation

PROFESSIONAL ELECTIVE III

23PVP206 DESIGN OF SEMICONDUCTOR MEMORIES **L T P C**
3 0 0 3

OBJECTIVES

- To study the architectures for SRAM and DRAM.
- To know about various non-volatile memories.
- To gain the knowledge about fault modeling and testing of memories for fault detection.
- To learn the radiation hardening process and issues for memory.
- To understand the fault modeling and testing procedures for memory circuit.

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES **9**

Static Random Access Memories (SRAMs):SRAM Cell Structures – MOS SRAM Architecture – MOS SRAM Cell and Peripheral Circuit Operation – Bipolar SRAM Technologies – Silicon On Insulator (SOI) Technology – Advanced SRAM Architectures and Technologies – Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development – CMOS DRAMs – DRAMs Cell Theory and Advanced Cell Structures – BiCMOS – DRAMS – Soft error failures in DRAMs – Advanced DRAM Designs and Architecture – Application, Specific DRAMs.

UNIT II NON VOLATILE MEMORIES **9**

Masked Read–Only Memories (ROMs) – High Density ROMs – Programmable Read –Only Memories (PROMs) – Bipolar PROMs – CMOS PROMs – Erasable (UV) – Programmable Read– Only Memories (EPROMs) – Floating – Gate EPROM Cell–One Time Programmable (OTP) EPROM – Electrically Erasable PROMs (EEPROMs) –EEPROM Technology and Architecture – Non volatile SRAM –Flash Memories(EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT III MEMORY FAULT MODELLING & TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE **9**

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing Application Specific Memory Testing. General Design for Testability Techniques – Ad Hoc Design Techniques, Structured Design Techniques – RAM Built-In Self – Test (BIST).

UNIT IV RELIABILITY AND RADIATION EFFECTS **9**

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability, Reliability Modeling and Failure Rate Prediction-Design for Reliability- Reliability Test Structures

Reliability creening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)- Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures**.**

UNIT V PACKAGING TECHNOLOGIES **9**

Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues- Memory Cards High Density Memory Packaging Future Directions.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Explain Static and Dynamic Memory structures.
- Examine the different RAM and ROM architecture and interconnects.
- Design and implement various fault modeling techniques in memory design.
- Discuss the type of memory for a specific application.
- Analyze the modeling for memory fault and testing.

TEXT BOOKS

1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability", PrenticeHall of India Private Limited, New Delhi, 2017.
2. Tegze P.Haraszti, "CMOS Memory Circuits", Kluwer Academic publishers, 2018.

REFERENCES

1. Betty Prince, "Emerging Memories: Technologies and Trends", Kluwer Academicpublishers, 2012.
2. Ivan Sutherland Bob Sproull, David Harris, "Logical Efforts, Designing Fast CMOSCircuits", Kluwr Academic Press, 2014.

E- RESOURCES

1. https://www.digimat.in/nptel/courses/video/108108122/L01l (Semiconductors)
2. https://nptel.ac.in/courses/108/108/108108112/ (Semiconductor memory)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	3	2	1	1	2	-	-	-	-	1	3	1	2	1
2	2	3	3	2	1	2	-	-	-	-	1	3	1	3	1
3	1	3	3	1	2	1	-	-	-	-	1	3	2	3	1
4	1	3	3	1	2	1	-	-	-	-	1	3	2	3	1
5	1	3	2	1	2	1	-	-	-	-	1	2	1	2	1
AVG	1.2	3.0	2.8	1.2	1.6	1.4	-	-	-	-	1.0	2.8	1.4	2.6	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP207 SCRIPTING LANGUAGES FOR VLSI L T P C
3 0 0 3

OBJECTIVES

- To study the scripting languages.
- To know about the security issues.
- To learn concept of TCL phenomena.
- To understand the concept of interfacing.
- To gain the knowledge of java script core language.

UNIT I INTRODUCTION TO SCRIPTING AND PERL 9

Characteristics of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT II ADVANCED PERL 9

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT III TCL 9

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT IV ADVANCED TCL 9

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running un trusted code, The C interface.

UNIT V TK AND JAVA SCRIPT 9

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze Scripting languages with arguments.
- Examine the concept of PERL.
- Evaluate the TCL structure, procedures.
- Illustrate the advanced of TCL.
- Discuss the TK and Java script.

TEXT BOOKS

1. Brent Welch,"Practical Programming in Tcl and Tk", Fourth Edition, 2015.
2. David Barron, "The World of Scripting Languages", Wiley Publications, 2017.

REFERENCES

1. Guido van Rossum, and Fred L. Drake ," Python Tutoria"l, Jr., editor, Release 2.6.4.
2. Randal L. Schwartz, "Learning PERL", sixth edition, O"Reilly.

E-RESOURCES

1. https://nptel.ac.in/courses/117/106/117106113/ (Linux Programming & Scripting)
2. http://nptelvideos.com/video.php?id=727(Computer Science)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	2	1	1	2	-	-	-	-	1	3	1	2	1
2	2	2	3	2	1	2	-	-	-	-	1	3	1	3	1
3	1	2	3	1	2	1	-	-	-	-	1	3	2	3	1
4	1	2	3	1	1	1	-	-	-	-	1	3	2	3	1
5	1	2	2	1	2	1	-	-	-	-	1	2	1	2	1
AVG	1.2	2.0	2.6	1.2	1.4	1.4	-	-	-	-	1.0	2.8	1.4	2.6	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP208 **NETWORKS ON CHIP** **L T P C**
3 0 0 3

OBJECTIVES

- To study the concept of network - on – chip.
- To learn router architecture designs.
- To acquire the fault tolerance network - on – chip.
- To gain knowledge test and fault tolerance of NOC.
- To understand an exposure on three-dimensional integration of network-on-chip.

UNIT I INTRODUCTION TO NOC **9**

Introduction to NoC –OSI layer rules in NoC - Interconnection Networks in Network-on- Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support.

UNIT II ARCHITECTURE DESIGN **9**

Switching Techniques and Packet Format - Asynchronous FIFO Design -GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design.

UNIT III ROUTING ALGORITHM **9**

Packet routing-Qos, congestion control and flow control – router design – network link design — Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms.

UNIT IV TEST AND FAULT TOLERANCE OF NOC **9**

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on-Chips.

UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP **9**

Three - Dimensional Networks-on-Chips Architectures. – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation for QoS On-Chip Communication – Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks- on-Chip.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the NOC and switching techniques.
- Examine different architecture design.
- Discuss different routing algorithms.
- Explain test and fault tolerance of NOC.
- Apply three-dimensional integration of network-on-chip.

TEXT BOOKS

1. ChrysostomosNicopoulos, Vijaykrishnan Narayanan, Chita R.Das, "Networks-on - Chip Architectures Holistic Design Exploration", Springer.
2. Fayezgebali, Haythamelmiligi, HqhahedWatheq E1-Kharashi "Networks-on-Chips theory and practice CRC press.

REFERENCES

1. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 2019.
2. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 2017.

E - RESOURCES

1. https://nptel.ac.in/courses/108/105/108105118/(Architectural Design of Digital integrated circuits)
2. https://nptel.ac.in/courses/106/105/106105183/(Computer Networks and Internet Protocol)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	-	1	3	-	-	-	-	-	-	1	3	1	2	1
2	1	-	1	3	-	-	-	-	-	-	1	3	2	3	1
3	1	-	1	3	-	-	-	-	-	-	1	2	2	3	1
4	1	-	1	1	-	-	-	-	-	-	1	2	2	3	1
5	1	-	1	1	-	-	-	-	-	-	1	2	1	2	1
AVG	1.0	-	1.0	2.2	-	-	-	-	-	-	1.0	2.4	1.6	2.6	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP209 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C
3 0 0 3

OBJECTIVES

- To know the sources affecting the speed of digital circuits.
- To gain knowledge multi-conductor transmission lines and cross-talk.
- To understand the analysis of non-ideal effects.
- To learn the methods of power considerations and system design.
- To study the clock distribution and clock oscillators.

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance, wave propagation, reflection, and bounce diagrams Reactive terminations — L, C, static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance, Transmission line losses – Rs, tan δ, routing parasitic, Common-mode current, differential-mode current, Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO, DC power bus design, layer stackup, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Examine the sources affecting the speed of digital circuits.
- Explain the multi-conductor transmission lines and cross-talk.
- Analyze the non-ideal signal effects.
- Illustrate the performance characteristics of power considerations and system design.
- Discuss the timing margin and clock jitter.

TEXT BOOKS

1. Douglas Brooks, "Signal Integrity Issues and Printed Circuit Board Design" Prentice Hall PTR, 2016.
2. Eric Bogatin, "Signal Integrity – Simplified", Prentice Hall PTR, 2018.

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 2019.
2. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley – Inter science, 2020.

E-RESOURCES

1. https://nptel.ac.in/courses/108/106/108106157/ (Transmission lines and electromagnetic waves)
2. https:// nptel.ac.in/courses/117/101/117101056/ (Introduction to EM waves and various techniques of communication)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	2	3	1	-	-	-	-	-	1	3	1	2	1
2	1	1	2	3	1	-	-	-	-	-	1	3	2	3	2
3	1	1	2	3	1	-	-	-	-	-	1	3	2	3	1
4	1	1	2	1	1	-	-	-	-	-	1	2	2	3	2
5	1	1	2	1	1	-	-	-	-	-	1	2	2	2	1
AVG	1.0	1.0	2.0	2.2	1.0	-	-	-	-	-	1.0	2.6	1.8	2.6	1.4

1-Low 2-Medium 3-High '-' – No Correlation

23PVP210	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L T P C 3 0 0 3

OBJECTIVES

- To understand Programmable Digital Signal Processor basics.
- To learn the TMS320C5X processor.
- To gain knowledge on the advanced DSP C6x architectures and some applications.
- To know the programmable ADSP's Architecture, addressing modes and instruction sets.
- To study Programming for signal processing applications.

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs **9**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II TMS320C5X PROCESSOR **9**

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation — Block Diagram of DSP starter kit — Application Programs for processing real time signals.

UNIT III TMS320C6X PROCESSOR **9**

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

UNIT IV ADSP PROCESSORS **9**

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V ADVANCED PROCESSORS **9**

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the fundamentals of DSP programming.
- Examine DSP TMS320C5X based System Developer.
- Analyze the concepts of C6x Digital Signal Processors.
- Discuss, compare and select the suitable Advanced DSP Processors for real-time signal processing applications.
- Discuss their ability to program the DSP processor for signal processing applications.

TEXT BOOKS

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx", cengage Learning India Private Limited, Delhi 2017.
2. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2019.

REFERENCES

1. Rulph Chassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A John Wiley & Sons, Inc., Publication, 2015.
2. User guides Texas Instrumentation, Analog Devices, Motorola.

E - RESOURCES

1. https://nptel.ac.in/courses/117/102/117102060/ (Digital Signal Processing)
2. https://nptel.ac.in/courses/108/106/108106149/ (Mapping Signal Processing Algorithms to Architectures)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	1	2	-	-	-	-	-	1	2	1	2	1
2	1	2	1	1	2	-	-	-	-	-	1	2	2	3	2
3	1	2	1	1	2	-	-	-	-	-	1	2	2	2	1
4	1	2	1	1	2	-	-	-	-	-	1	2	1	2	2
5	1	2	1	1	2	-	-	-	-	-	1	2	1	2	1
AVG	1.0	2.0	1.0	1.0	2.0	-	-	-	-	-	1.0	2.0	1.4	2.2	1.4

1-Low 2-Medium 3-High '-' – No Correlation

PROFESSIONAL ELECTIVE IV

23PVP301 MIXED SIGNAL VLSI DESIGN L T P C
3 1 0 4

OBJECTIVES

- To understand the concepts of switched capacitor circuits.
- To study the concepts of phase lock loops.
- To learn the data converter fundamentals.
- To acquire the knowledge about the A/D converters.
- To gain the knowledge of sampling converters.

UNIT I SWITCHED CAPACITOR CIRCUITS 9+3

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, Biquad filters.

UNIT II PHASED LOCK LOOP (PLL) 9+3

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT III DATA CONVERTER FUNDAMENTALS 9+3

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based Converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT IV NYQUIST RATE A/D CONVERTERS 9+3

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D Converters, Folding A/D converters, Pipelined A/D converters, Time-Interleaved Converters.

UNIT V OVERSAMPLING CONVERTERS 9+3

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss the knowledge of Switched Capacitor Circuits.
- Analyze the concepts of Phased Lock Loop.
- Apply appropriate techniques, resources and tools to engineering activities in developmentof Data Converters.
- Examine the engineering problems with wide range of solutions to increase Data Rate of ADCand DAC.
- Illustrate nose shaping modulators.

TEXT BOOKS

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH Edition, 2015.
2. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, International second Edition/Indian Edition, 2016.

REFERENCES

1. Rudy Van De Plassche, "CMOS Integrated Analog-to-Digital and Digital-to Analog converters", Kluwer Academic Publishers, 2020.
2. Richard Schreier, "Understanding Delta-Sigma Data converters", Wiley Inter science, 2015.

E - RESOURCES

1. https://nptel.ac.in/courses/117/106/117106034/(VLSI Data Conversion Circuits)
2. https://nptel.ac.in/courses/108/106/108106084/(Analog Circuits)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	1	2	2	-	-	-	-	1	2	1	2	1
2	1	2	1	1	2	2	-	-	-	-	1	2	1	3	2
3	1	2	1	1	2	2	-	-	-	-	1	2	1	2	1
4	1	2	1	1	2	2	-	-	-	-	1	2	1	2	2
5	1	2	1	1	2	2	-	-	-	-	1	2	1	2	1
AVG	1.0	2.0	1.0	1.0	2.0	2.0	-	-	-	-	1.0	2.0	1.0	2.2	1.4

1-Low 2-Medium 3-High '-' – No Correlation

23PVP302 **EMBEDDED SYSTEM DESIGN** **L T P C**
3 1 0 4

OBJECTIVES

- To acquire knowledge of general embedded system and design methodology.
- To learn about the ASIPs and UART.
- To understand the basic concept of protocols and bus structures.
- To Study state machine and concurrent process models.
- To gain the knowledge on embedded software development tools and RTOS.

UNIT I EMBEDDED SYSTEM OVERVIEW **9+3**

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT- Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR **9+3**

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer"s view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to- Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES **9+3**

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS **9+3**

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS **9+3**

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Examine the Embedded System Overview.
- Analyze general and single purpose processor.
- Explain the different type of protocols.
- Discuss state machine and design process models.
- Illustrate the embedded software development tools and RTOS.

TEXT BOOKS

1. Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", Third edition, Pearson Education, 2019.
2. Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2022.

REFERENCES

1. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons,2016.
2. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2019.

E - RESOURCES

1. https://nptel.ac.in/courses/108/102/108102169/(Introduction to Embedded SystemDesign)
2. https://nptel.ac.in/courses/106/105/106105159/(Embedded Systems Design)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	2	2	3	1	-	-	-	-	1	3	1	2	1
2	1	1	2	2	3	1	-	-	-	-	1	3	1	2	2
3	1	1	2	2	3	1	-	-	-	-	1	3	1	2	1
4	1	1	2	2	3	1	-	-	-	-	1	3	1	2	1
5	1	1	2	2	3	1	-	-	-	-	1	3	1	2	1
AVG	1.0	1.0	2.0	2.0	3.0	1.0	-	-	-	-	1.0	3.0	1.0	2.0	1.2

1-Low 2-Medium 3-High '-' – No Correlation

23PVP303 SOFT COMPUTING AND OPTIMIZATION TECHNIQUES L T P C
3 1 0 4

OBJECTIVES

- To study the design of various neural networks.
- To learn the concept of fuzzy logic.
- To gain insight onto Neuro Fuzzy modeling and control.
- To acquire the Knowledge in conventional optimization techniques.
- To understand the various evolutionary optimization techniques.

UNIT I NEURAL NETWORKS 9+3

Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network.

UNIT II FUZZY LOGIC 9+3

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making.

UNIT III NEURO-FUZZY LOGIC MODELING 9+3

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro-Fuzzy Control – Case Studies.

UNIT IV CONVENTIONAL OPTIMIZATION TECHNIQUES 9+3

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton"s Method, Marquardt Method, Constrained optimization –sequential linearprogramming, Interior penalty function method, external penalty function method.

UNIT V EVOLUTIONARY OPTIMIZATION TECHNIQUES 9+3

Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Illustrate machine learning through neural networks.
- Explain a Fuzzy expert system.
- Examine Neuro Fuzzy system for clustering and classification.
- Analyze the optimization techniques to solve the real world problems.
- Discuss various Soft computing frameworks.

TEXT BOOKS

1. David E. Goldberg, "Genetic Algorithms in Search, Optimization and Machine Learning", Addison wesley, 2019.
2. Singiresu S. Rao, "Engineering optimization Theory and practice", John Wiley & sons, inc, fourth Edition, 2019.

REFERENCES

1. Venkata Rao, Vimal J. Savsani, Mechanical Design Optimization Using Advanced OptimizationTechniques, springer 2016.
2. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice Hall of India, 2018.

E-RESOURCES

1. https://nptel.ac.in/courses/106/105/106105173/(Introduction to Soft Computing)
2. https://nptel.ac.in/courses/117/105/117105084/(Neural Networks and Applications)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	-	2	1	2	-	-	-	-	-	1	2	1	2	1
2	1	-	2	1	2	-	-	-	-	-	1	2	2	2	1
3	1	-	2	1	2	-	-	-	-	-	1	2	2	2	1
4	1	-	2	1	2	-	-	-	-	-	1	2	2	2	1
5	1	-	2	1	2	-	-	-	-	-	1	2	1	2	1
AVG	1.0	-	2.0	1.0	2.0	-	-	-	-	-	1.0	2.0	1.4	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP304 **VLSI FOR BIOMEDICAL SYSTEMS** **LT P C**
3 1 0 4

OBJECTIVES

- To learn the concept of biomedical sensing.
- To know the Wireless implantable devices.
- To understand the CMOS circuits for wireless medical applications.
- To acquire the knowledge of solid state interface and neural stimulation.
- To study about the neuron models and CMOS systems.

UNIT I BIO MEDICAL SENSING **9+3**

Neuro chemical sensing-Neuro potential sensing- RF telemetry and Power harvesting in Implant devices- Multimodal Electrical and Chemical Sensing-Prosthesis exterior body unit and wireless link-Body implantable unit- system prototype.

UNIT II CMOS CIRCUITS FOR BIOMEDICAL IMPLANTABLE DEVICES **9+3**

Inductive link to deliver power implants- Data transmission through inductive links- Energy and Bandwidth issues in multi-channel recording- Strain Measurement and motivation for self-power sensing-Piezoelectric transduction and power delivery- Micro watt piezo powered electric circuits-Design and calibration of floating gate sensor Array.

UNIT III CMOS CIRCUITS FOR WIRELESS MEDICAL APPLICATIONS **9+3**

Spectrum usage for medical Use- integrated transmitter and receiver architectures- radio architecture selection- Low noise amplifiers- Mixers-Poly phase filters -Power Amplifiers and PLL.

UNIT IV SOLID STATE INTERFACE AND NEURAL STIMULATION **9+3**

Micro needles – Types, Fabrication, Drug delivery and biosensing- Neural signal Recording and Amplifications-Neuro chemical Recording. Electrode configuration and tissue volume conductor, Electrode- Electrolyte interface- Efficacy of Neural simulation - Stimulus generator architecture, Stimulation of front end circuits- Bioamplifier circuits and stimulation.

UNIT V NEUROMEMITIC IC, AND LABEL FREE DIAGNOSTICS **9+3**

Neuron models for cell and network level- criteria and design strategies of nueromemitic IC - Fixed and Tunable model circuits. Label free molecular detection- Electrodes bio-functionalization, Bio chip application for DNA- Architectural optimizations for Digital Microfluidic biochips- Magnetotatic bacteria as the functional component in CMOS microelectronic Systems.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Examine the Concept of Neural activity of the brain
- Apply CMOS circuits for Implantable devices.
- Analyze the use of Wireless technology in medical devices.
- Design and analyze the Micro needle fabrication.
- Illustrate the Biochip for Biomedical Applications.

TEXT BOOKS

1. Krzysztof Iniewski, "VLSI Circuits for Biomedical Applications" Artech house Inc. 2018.
2. Rahul Sarpeshkar, "Ultra Low Power Bioelectronics: Fundamentals,Biomedical Applications and Bio-inspired Systems", Cambridge University Press, 2017.

REFERENCES

1. E. Sanchez-Sinencio and A. G. Andreau "Low-voltage/Low-power Integrated Circuits and Systems", Wiley,2015.
2. Khandpur RS, "Handbook of Biomedical Instrumentation", McGraw Hill, New Delhi,2018.

E- RESOURCES

1. https://nptel.ac.in/courses/102/107/102107058/(Biomedical)
2. https://nptel.ac.in/noc/courses/noc20/sem1/noc20-ee44/ (Bio medical application)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	1	1	-	-	-	-	-	1	-	1	2	1
2	1	1	1	1	1	-	-	-	-	-	1	-	1	2	1
3	1	1	1	1	1	-	-	-	-	-	1	-	1	2	1
4	1	2	1	1	1	-	-	-	-	-	1	-	1	2	1
5	1	2	1	1	1	-	-	-	-	-	1	-	1	2	1
AVG	1.0	1.6	1.0	1.0	1.0	-	-	-	-	-	1.0	-	1.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP305 **RF IC DESIGN** **L T P C**
3 1 0 4

OBJECTIVES

- To learn the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs.
- To know the active and passive mixers.
- To study the tuning range of different oscillator circuits.
- To gain the knowledge of PLL and frequency synthesizers.

UNIT I IMPEDANCE MATCHING IN AMPLIFIERS **9+3**

Definition of „Q", series parallel transformations of lossy circuits, impedance matching using „L",„PI" and T networks, Integrate Inductors, Resistors, Capacitors, tunable inductors, transformers.

UNIT II AMPLIFIER DESIGN **9+3**

Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design.

UNIT III ACTIVE AND PASSIVE MIXERS **9+3**

Qualitative Description of the Gilbert Mixer - Conversion Gain, and distortion and noise , analysis of Gilbert Mixer - Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV OSCILLATORS **9+3**

LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS **9+3**

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss the principles of operation of an RF receiver front end and be able to design and apply constraints for LNAs, Mixers and Frequency synthesizers.
- Illustrate the Radio Frequency Integrated Circuits.
- Analyze complex engineering problems critically for conducting research in RF systems.
- Explain the engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
- Apply appropriate techniques to engineering activities in the field of RF IC Design.

TEXT BOOKS

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,2021.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 2017.

REFERENCES

1. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2016.
2. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits", Cambridge University Press, 2017.

E-RESOURCES

1. https://nptel.ac.in/courses/117/102/117102012/#(RF Integrated Circuits)
2. https://nptel.ac.in/courses/117/106/117106030/#(Analog IC Design)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	2	1	2	2	2	-	-	-	-	-	1	2	1	2	1
2	2	1	2	2	2	-	-	-	-	-	1	2	1	2	1
3	1	2	2	2	2	-	-	-	-	-	1	2	1	2	2
4	1	2	2	2	2	-	-	-	-	-	1	2	1	2	2
5	2	2	2	3	2	-	-	-	-	-	1	2	1	2	1
AVG	1.6	1.6	2.0	2.2	2.0	-	-	-	-	-	1.0	2.0	1.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

PROFESSIONAL ELECTIVE V

23PVP306 HARDWARE VERIFICATION TECHNIQUES L T P C
3 1 0 4

OBJECTIVES

- To learn about constrained random verification methods.
- To study code coverage and functional coverage.
- To acquire assertion based verification of high level modeling.
- To understand the self checking test benches.
- To gain the knowlege concept of Verification using UVM.

UNIT I VERIFICATION TECHNOLOGIES 9+3

Importance of verification - reconvergence model-the human factor- formal and functional verification approaches –timing verification –testing versus verification-design and verification reuse-linting.

UNIT II VERIFICATION TOOLS 9+3

Simulation-third party models-verification-intellectual property-waveform viewers-code coverage-functional coverage-issue tracking-metrics-roles of the verification plan –levels of verification — verification strategies.

UNIT III HIGH LEVEL MODELING 9+3

High level versus RTL thinking-Structure of high level code-data abstraction-object oriented programming-parallel simulation engine-race issues-portability issues.

UNIT IV TEST CASE GENERATION AND ARCHITECTING TESTBENCHES 9+3

Simple stimulus-simple output-complex stimulus-bus functional models -response monitors-transaction level Interface-verification harness- design configuration-self checking test benches-directed stimulus-random stimulus- system level verification harness — transaction level models — managing stimulation-regression.

UNIT V VERIFICATION METHODOLOGY 9+3

Universal Verification Methodology (UVM) – packages -components – Environmental structures factory registration – reporting.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the verification strategies.
- Discuss the structure of high level code.
- Examine the high level versus RTL thinking.
- Design self checking test benches.
- Explain the procedure for factory registration and reporting.

TEXT BOOKS

1. Chris Spear, Greg Tumbush, "System verilog for verification-A Guide to Learning thebest Language Features" Springer Third edition, 2019.
2. Kropf T, "Introduction to Formal Verification Technique" Springer verilog, 2015.

REFERENCES

1. Janick Bergeron, "Writing Test Benches Using System Verilog", Springer First Edition, 2019.
2. Mark Glasser, "Open Verification Methodology Cookbook", Springer Verilog, 2016.

E- RESOURCES

1. https://nptel.ac.in/courses/117/103/117103125/ (VLSI Design verification and test)
2. https://nptel.ac.in/courses/106/103/106103116/ (Test of Digital VLSI circuits)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	-	2	2	-	-	-	-	-	-	1	2	1	2	1
2	1	-	2	2	-	-	-	-	-	-	1	2	1	2	1
3	1	-	2	2	-	-	-	-	-	-	2	3	1	2	2
4	1	-	2	2	-	-	-	-	-	-	2	2	1	2	2
5	1	-	2	2	2	-	-	-	-	-	1	3	1	2	1
AVG	1.0	-	2.0	2.0	2.0	-	-	-	-	-	1.4	2.4	1.0	2.0	1.4

1-Low 2-Medium 3-High '-' – No Correlation

23PVP307 **VLSI FOR WIRELESS COMMUNICATION** **L T P C**
3 1 0 4

OBJECTIVES

- To understand the concepts of power amplifier.
- To study the Transmitter and receiver architectures of VLSI for wireless Communication.
- To understand the various types of mixers designed for wireless communication.
- To know the application of frequency synthesizers.
- To gain the basic Knowledge of receiver architecture.

UNIT I OVERVIEW OF WIRELESS COMMUNICATION SYSTEMS **9+3**

Introduction of wireless system, Low Noise Amplifier – Matching Network, Wideband LNA –DC Bias-Gain and frequency Response-Noise Figure, Narrowband LNA - Impedance Matching-Matching of Imaginary and real Part-Interpretation of Power Matching, Core Amplifiers-Noise Figure-Power Dissipation, Trade- Off and Noise contribution from Other Sources.

UNIT II TRANSMITTER ARCHITECTURE AND POWER AMPLIFIER **9+3**

Transmitter Back End, Quaderature LO generator-Single ended RC and LC, R-C with Differential stages Polyphase IQ generator-Divider based generator, Power Amplifier Design.

UNIT III MIXERS **9+3**

Active Mixer: Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Analysis of Gilbert Mixer of Low Frequency Case and High-Frequency Case - Noise. Passive Mixer: Switching Mixer–Distortion, Conversion Gain and Noise in Unbalanced Switching, Conversion Gain, Sampling Mixture, Gain, Distortion and noise in Single Ended Sampling Mixer.

UNIT IV FREQUENCY SYNTHESIZER **9+3**

Phase Locked Loops - Phase Detector - VCO - Dividers - LC Oscillators - Ring Oscillators - Phase Noise – Loop Filter-First order filter-Second order filter, High Order filter, Digital Enhanced Cordless Telecommunication.

UNIT V RECEIVER ARCHITECTURE **9+3**

Receiver Front end-Filter Design-Band selection Filter, Image Rejection Filter, Channel Filter, Restof receiver front end- non idealities and design parameters, Derivation of Noise Figure(NF) and input third order Intercept points(IIP3) of receiver front end, Partitioning of required NF and IIP3 ofreceiver front end into individual NF and IIP3.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss the Low Noise Amplifier which includes wideband, narrow band for impedance matching and Core Amplifier.
- Illustrate the Transmitter Architectures and Power Amplifier.
- Examine the types of mixer and its parameters.
- Explain the application of frequency synthesizers.
- Analyze the Receiver Architectures.

TEXT BOOKS

1. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, second edition,2020.
2. Carols and M. Stewart, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Publication, 2016.

REFERENCES

1. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits',Cambridge University Press , 2018.
2. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kluwer Academic Publishers, 2020.

E - RESOURCES

1. https://nptel.ac.in/courses/117/102/117102012/ (Power Amplifiers)
2. https://nptel.ac.in/courses/117/102/117102062/ (Wireless Communication)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	3	2	1	1	-	-	-	-	1	-	1	2	1
2	1	2	3	2	1	1	-	-	-	-	1	-	1	2	1
3	1	2	3	2	1	1	-	-	-	-	1	-	1	2	1
4	1	2	3	2	1	1	-	-	-	-	1	-	1	2	1
5	1	2	3	2	2	1	-	-	-	-	1	-	1	2	1
AVG	1.0	2.0	3.0	2.0	1.2	1.0	-	-	-	-	1.0	-	1.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP308 **ASIC DESIGN** **L T P C**
3 1 0 4

OBJECTIVES

- To study the types of ASIC and ASIC Library Design.
- To gain knowledge on Programmable ASICS.
- To learn programming ASIC design software and Low-Level Design Entry.
- To understand the architecture of different types routing.
- To know the high performance algorithms for ASICS.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9+3

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell — Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9+3

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - XilinxI/O blocks**.**

UNIT III PROGRAMMABLE ASIC ARCHITECTURE 9+3

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9+3

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V HIGH PERFORMANCE ALGORITHMS FOR ASICS/ SOCS.SOC CASE STUDIES 9+3

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon Completion of the course, Students will be able to

- Examine the passive elements for ASIC design Analyze the characteristics of Programmable ASIC I/O cells.
- Analyze the synthesis part on different logic structures.
- Illustrate the programmable ASIC architecture.
- Discuss the physical design flow of ASIC.
- Analyze high performance algorithms available for ASICs.

TEXT BOOKS

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2021.
2. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2019.

REFERENCES

1. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers,2020.
2. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs).Prentice Hall PTR, 2019.

E – RESOURCES

1. https://nptel.ac.in/courses/117/106/117106092/(Asic design)
2. https://nptel.ac.in/courses/108/106/108106177/(Digital Design)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	1	2	3	1	-	-	-	-	1	2	1	2	1
2	1	1	1	2	3	1	-	-	-	-	1	2	1	2	2
3	1	1	1	2	3	1	-	-	-	-	1	2	1	2	2
4	1	1	1	2	3	1	-	-	-	-	1	2	1	2	2
5	1	1	1	2	3	1	-	-	-	-	1	2	1	2	1
AVG	1.0	1.0	1.0	2.0	3.0	1.0	-	-	-	-	1.0	2.0	1.0	2.0	1.6

1-Low 2-Medium 3-High '-' – No Correlation

23PVP309 **NANO SCALE DEVICES** **L T P C**
3 1 0 4

OBJECTIVES

- To understand about multi-gate devices.
- To learn the concepts of Multigate MOS systems.
- To know the various nano wire FETs.
- To understand the radiation effects in MOSFETS.
- To study nano-scaled MOS transistors with the physical insight of their functional characteristic.

UNIT I INTRODUCTION TO NOVEL MOSFETS **9+3**

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility– threshold voltage – inter subband scattering, multigate technology – mobility – gate stack.

UNIT II PHYSICS OF MULTIGATE MOS SYSTEMS **9+3**

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility.

UNIT III NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE **9+3**

Silicon nano wire MOSFETs -Evaluvation of I-V characteristics — The I-V characteristics for nondegenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs –Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels– Molecular transistors – Single electron charging – Single electron transistors.

UNIT IV RADIATION EFFECTS **9+3**

Radiation effects in SOI MOSFETs, total ionizing dose effects — single gate SOI — multigate devices, single event effect, scaling effects**.**

UNIT V CIRCUIT DESIGN USING MULTIGATE DEVICES **9+3**

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance -intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon Completion of the course, Students will be able to:

- Design circuits using nano scaled MOS transistors with the physical insight of their functional characteristics.
- Understand and study the physics behind the operation of multi-gate systems
- Examine the MOS devices used below 10nm and beyond with an eye on the future.
- Analyze the radiation effects in MOSFETS.
- Discuss the present and future research frontiers of Nano electronics and to be able to critically assess future trends.

TEXT BOOKS

1. J.P.Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2018.
2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2016.

REFERENCES

1. M.S.Lundstorm, "Fundamentals of Carrier Transport", second Ed., Cambridge University Press,Cambridge UK, 2021.
2. Handbook of Nanofabrication: Editor Gary P. Wiederrecht, Elsevier Publication, Academic Press, 2019.

E-RESOURCES

1. https://nptel.ac.in/courses/117/108/117108047/ (Nano Electronics Device and Materials)
2. https://nptel.ac.in/courses/108/101/108101089/ (VLSI circuits using MOS Technology)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	1	-	-	-	-	-	-	2	2	1	2	1
2	1	2	1	1	-	-	-	-	-	-	2	1	1	2	2
3	1	2	1	1	-	-	-	-	-	-	2	1	1	2	2
4	1	2	1	1	-	-	-	-	-	-	1	1	1	2	2
5	1	2	1	1	-	-	-	-	-	-	1	2	1	2	1
AVG	1.0	2.0	1.0	1.0	-	-	-	-	-	-	1.6	1.4	1.0	2.0	1.6

1-Low 2-Medium 3-High '-' – No Correlation

23PVP310 **IP BASED VLSI DESIGN** **L T P C**
3 1 0 4

OBJECTIVES

- To learn about IC manufacturing and fabrication.
- To know the combinational networks design.
- To understand sequential and subsystem design.
- To study about different floor planning techniques and architecture design.
- To acquire the knowledge about IP design security.

UNIT I VLSI AND ITS FABRICATION **9+3**

Introduction, IC manufacturing, CMOS technology, IC design techniques, IP based design, Fabrication process-Transistors, Wires and Via, Fabrication Theory reliability, Layout Design and tools.

UNIT II COMBINATIONAL LOGIC NETWORKS **9+3**

Logic Gates: Combinational Logic Functions, Static Complementary Gates, Switch Logic, Alternate Gate circuits, Low power gates, Delay, Yield, Gates as IP, Combinational Logic Networks- Standard Cell based Layout, Combinational network delay, Logic and Interconnect design, Power optimization, Switch logic network, logic testing.

UNIT III SUBSYSTEM DESIGN **9+3**

Sequential Machine-Latch and Flip flop, System design and Clocking, Performance analysis, power optimization, Design validation and testing; Subsystem Design-Combinational Shifter, Arithmetic Circuits, High Density memory, Image Sensors, FPGA,PLA, Buses and NoC, Datapaths, Subsystems as IP.

UNIT IV FLOOR PLANNING AND ARCHITECTURE DESIGN **9+3**

Floor planning-Floor planning methods, Global Interconnect, Floor plan design, Off-chip Connections Architecture Design- HDL, Register-Transfer Design, Pipelining, High Level Synthesis, Architecture for Low power, GALS systems, Architecture Testing, IP Components, Design Methodologies, Multiprocessor System-on-chip Design.

UNIT V DESIGN SECURITY **9+3**

IP in reuse based design, Constrained based IP protection, Protection of data and Privacy constrained based watermarking for VLSI IP based protection.

TOTAL: 45+15=60 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Illustrate the IP based design techniques.
- Discuss about the combinational logic gates.
- Analyze the subsystem design.
- Examine the floor planning methods.
- Design the security systems.

TEXT BOOKS

1. Wayne wolf, "Modern VLSI Design: IP-based Design", Pearson Education,2019.
2. Qu gang, Miodrag potkonjak, "Intellectual Property Protection in VLSI Designs: Theory and Practice", kluwer academic publishers, 2020.

REFERENCES

1. Sorab K. Ghand," VLSI Fabrication Principles: Silicon and Gallium Arsenide", second Edition,2016.
2. Khaled Salah Mohamed " IP Cores Design from Specifications to Production: Modeling, Verification, Optimization, and Protection (Analog Circuits and Signal Processing)" first Edition, Kindle Edition, 2016.

E-RESOURCES

1. https://nptel.ac.in/courses/108/107/108107129/ (Combinational Logic Design)
2. https://nptel.ac.in/courses/113/106/113106062/ (IC Device fabrication)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	3	2	1	-	-	-	-	1	2	1	3	1
2	2	2	1	3	2	1	-	-	-	-	1	1	2	3	2
3	2	2	1	3	2	1	-	-	-	-	1	1	2	3	2
4	2	1	1	3	1	1	-	-	-	-	1	1	2	2	2
5	1	1	1	3	1	1	-	-	-	-	1	2	2	2	1
AVG	1.0	1.0	1.0	3.0	1.6	1.0	-	-	-	-	1.0	1.4	1.8	2.6	1.6

1-Low 2-Medium 3-High '-' – No Correlation

PROFESSIONAL ELECTIVE VI

23PVP311 **VLSI FOR IOT SYSTEMS** **L T P C**
3 0 0 3

OBJECTIVES

- To study the concepts of IoT Systems.
- To know the Components of IoT.
- To learn the fabrication of IC technology.
- To understand the Electronic system design for IoT.
- To gain the knowledge of IoT systems.

UNIT I INTRODUCTION **9**

Concept of connected world, Need, Legacy systems for connected world, features and limitations, key features of IoT architecture, Merits and Demerits of IoT Technology, Applications driven by IoT technology, examples.

UNIT II COMPONENTS OF IOT **9**

Review of classic embedded system architecture ,Basic building blocks of an IoT system, Artificial Intelligence, Connectivity, Sensors and computing nodes. Sensors used in IoT Systems, Characteristics and requirements, Types of sensors for IoT systems, Compute nodes of IoT, Connectivity technologies in IoT, Software in IoT systems, features and properties.

UNIT III IC TECHNOLOGY FOR IOT **9**

SoC Architecture for IoT devices, Application processor, microcontrollers, smart analog, memory architecture for IoT, Non volatile memories(NVM),Embedded non volatile memories, Anti-fuse one time programmable(OTP) memories, Power management, Low drop out regulators, DC-to DC Converters, Voltage References, Power Management Units(PMUs) in IC's and Systems, Role of Field Programmability in IoT systems.

UNIT IV ELECTRONIC SYSTEM DESIGN FOR IOT **9**

Electronic system Design for IoT, Requirements, Computing blocks in IoT systems, MCU's, DSPs and FPGA's, System power supply design for IoT systems, Mixed signal challenges in hardware systems, Form Factor, Guidelines and prevailing standards.

UNIT V ANALYSIS OF IOT SYSTEMS **9**

Component models and System Design, Feasibility and challenges, System level integration, Operating conditions of IoT devices and impact on Electronic System design, hardware security issues, EMI/EMC, SI/PI and Reliability analysis in IoT systems.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Analyze the concepts of VLSI IoT systems.
- Examine the Components of IoT.
- Develop the IC technology for IoT.
- Illustrate of Electronic system design.
- Examine the Component models and system design.

TEXT BOOKS

1. Alloto,"Enabling the internet of Things from Integrated Circuits to Integrated systems",SpringerPublications, first Edition,2017.
2. Pieter Harpe,Kofi A,A makinwaAndrea Baschirotto, " Hybrid ADCs,Smart sensors for the IoT,and sub-1V& Advanced Node analog circuit Design",Springer International Publishing AG,2017.

REFERENCES

1. Rashid khan,Ajith vasudevan,"Learning IoT with Particle Photon and Electron",Packt PublishingLimited(Verlag),2016.
2. ApekMulay, "Sustaining Moore's Law: Uncertainty Leading to a certainty of IoT Revolution",Margan and Claypool Publishers,2015.

E-RESOURCES

1. https://nptel.ac.in/courses/108/108/108108111/ (Introduction of IC)
2. https://www.digimat.in/nptel/courses/video/108101089/l21.html (Fabrication of MOS)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	2	2	1	3	-	-	-	-	2	3	3	3	3
2	3	3	2	2	1	-	-	-	-	-	1	2	3	3	3
3	3	3	3	2	1	2	-	-	-	-	3	2	3	2	3
4	3	3	2	2	3	-	-	-	-	-	2	1	3	3	2
5	3	2	3	3	2	1	-	-	-	-	-	1	3	2	2
AVG	3.0	2.4	2.4	2.2	1.6	1.2	-	-	-	-	1.6	1.8	3.0	2.6	2.6

1-Low 2-Medium 3-High '-' – No Correlation

23PVP312 VLSI ARCHITECTURE FOR IMAGE AND VIDEO PROCESSING **L T P C**
3 0 0 3

OBJECTIVES

- To gain the knowledge of Image and Video processing algorithms.
- To study the various processing techniques of Image and Video signals.
- To learn the different architectures of Image and Video signals.
- To know Fast Motion Estimation Algorithms.
- To understand various VLSI architectures for video processing

UNIT I IMAGE PROCESSING ALGORITHMS **9**

Introduction - Image Processing Tasks - Low level Image Processing Operations – Description of some intermediate level operations – Requirements for Image processor architecture.

UNIT II IMAGE PROCESSING ARCHITECTURES AND PIPELINED LOW LEVEL IMAGE PROCESSING **9**

Classification of architecture – Uni and Multi processors – MIMD systems – SIMD systems – pipelines – Devices for cellular logic processing – Design aspects of real time low level image processors – Design method for special architectures.

UNIT III TPIPELINED ARCHITECTURES & 2D AND 3D IMAGE PROCESSING ARCHITECTURES **9**

Architecture of a cellular logic processing element – Second decomposition in data path and control –Real time pipeline for low level image processing – Design aspects of Image Processing architectures Implementation of Low level 2D and 3D and Intermediate level algorithms.

UNIT IV VIDEO PROCESSING ALGORITHMS **9**

Motion Estimation Algorithms – Complexity Analysis Methodology – Complexity analysis of MPEG 4 Visual – Analysis of Fast Motion Estimation Algorithms.

UNIT V VLSI ARCHITECTURES FOR VIDEO PROCESSING **9**

General design space evaluation – Design space motion estimation architectures – Motion estimation architectures for MPEG-4 – Design Trade-offs – VLSI implementation search engine land search engine II.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Discuss the various architectures to realize Image processing algorithms.
- Analyze the pipeline architectures for image processing.
- Explain the Low level 2D and 3D and Intermediate level algorithms.
- Discuss the performances of video processing algorithms.
- Illustrate the various architectures for video Processing.

TEXT BOOKS

1. Peter M. Kuhn, "Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation ", Springer ISBN 978-1–4419-5088-8, first^{t} edition, 2015.
2. Pieter Jonker, "Morphological Image Processing: Architecture and VLSI design",Springer. ISBN:9020127667, first edition, 2020.

REFERENCES

1. Rafael C. Gonzalez & Richard E. Woods, "Digital Image Processing", Prentice Hall; third edition, 2017.
2. A.Murat Tekalp, "Digital Video Processing", Pearson Education, Noida, first edition, 2015.

E-RESOURCES

1. https://nptel.ac.in/courses/117/105/117105135/(Image Processing).
2. https://nptel.ac.in/courses/117/105/117105079/ (Digital Image Processing).

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	1	1	-	-	-	-	-	2	-	3	2	3
2	1	2	1	1	1	-	-	-	-	-	1	-	3	2	3
3	1	2	1	1	1	-	-	-	-	-	3	-	3	2	3
4	1	1	1	1	1	-	-	-	-	-	2	-	3	2	2
5	1	1	1	1	1	-	-	-	-	-	-	-	3	2	2
AVG	1.0	1.6	1.0	1.0	1.0	-	-	-	-	-	1.6	-	3.0	2.0	2.0

1-Low 2-Medium 3-High '-' – No Correlation

23PVP313 **HARDWARE - SOFTWARE CO-DESIGN** **L T P C**
3 0 0 3

OBJECTIVES

- To acquire knowledge about system specification and modeling.
- To know the design of hardware/software partitioning.
- To understand the concepts of hardware/software co-synthesis.
- To study the different technical aspects about prototyping and emulation.
- To gain the knowledge of design specification and verification.

UNIT I SYSTEM SPECIFICATION AND MODELLING **9**

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE / SOFTWARE PARTITIONING **9**

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE / SOFTWARE CO-SYNTHESIS **9**

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

UNIT IV PROTOTYPING AND EMULATION **9**

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data- Dominated Systems ,Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION **9**

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification ,Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi- Language Co- simulation.

TOTAL: 45 PERIODS

OUTCOMES

Upon Completion of the course, Students will be able to

- Explain the concepts of system specification and modeling.
- Analyze the hardware/software partitioning.
- Discuss hardware / software co-synthesis.
- Illustrate prototyping and emulation technique.
- Examine the design specification and validate its functionality by simulation.

TEXT BOOKS

1. Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design"Kaufmann Publishers, 2018.
2. Jorgen Staunstrup, Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" ,Kluwer Academic Pub,2019.

REFERENCES

1. Ralf Niemann , "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 2017.
2. F.Balarin, Chiodo"Hardware/Software Co-Design of Embedded Systems", Kluwer Academic Pub, 2016.

E- RESOURCES

1. https://onlinecourses.nptel.ac.in/noc20_cs14 (Embeeded design)
2. https://nptel.ac.in/courses/108/108/108108157/ (electronics prototype buliding)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	2	2	-	1	-	-	-	-	2	2	1	2	3
2	1	1	2	2	-	1	-	-	-	-	1	1	1	2	3
3	1	1	2	2	-	1	-	-	-	-	3	1	1	2	3
4	1	1	2	2	2	1	-	-	-	-	2	1	3	2	2
5	1	1	2	2	2	1	-	-	-	-	1	2	3	2	2
AVG	1.0	1.0	2.0	2.0	2.0	1.0	-	-	-	-	1.8	1.4	1.9	2.0	2.6

1-Low 2-Medium 3-High '-' – No Correlation

23PVP314 **SELECTED TOPICS IN IC DESIGN** **L T P C**
3 0 0 3

OBJECTIVES

- To gain the knowledge the concepts of voltage and current references.
- To learn about the low drop out regulators.
- To understand the oscillator fundamentals.
- To study the concepts of phase lock loops.
- To acquire the knowledge on clock and data recovery.

UNIT I VOLTAGE AND CURRENT REFERENCES **9**

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing.

UNIT II LOW DROP OUT REGULATORS **9**

Analog Building Blocks, Negative Feedback, AC Design, Noise and Noise Reduction Techniques, Stability, LDO Efficiency, LDO Current Source, LDO Current Source Using Opamp.

UNIT III OSCILLATOR FUNDAMENTALS **9**

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV PHASE LOCK LOOPS **9**

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance.

UNIT V CLOCK AND DATA RECOVERY **9**

CDR Architectures, TIAs and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

OUTCOMES

Upon Completion of the course, Students will be able to

- Examine the basics of voltage and current references.
- Design the low drop out regulators.
- Apply basic knowledge of oscillator fundamentals.
- Explain the skill to phase lock loops.
- Discuss the CDR architectures.

TEXT BOOKS

1. Behzad Razavi, "Design of Integrated circuits for Optical Communications", McGraw Hill,2020.
2. Floyd M. Gardner ,"Phase Lock Techniques" John Wiley & Sons, Inc 2015.

REFERENCES

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher orderbandgapcircuits", John Wiley and Sons, Inc 2022.
2. High Speed Clock and Data Recovery, High-performance Amplifiers Power ManagementSpringer, 2018.

E - RESOURCES

1. https://nptel.ac.in/courses/108/106/108106158/ (Digital IC Design)
2. https://onlinecourses.nptel.ac.in/noc21_ee22/preview (IC Design)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	2	1	2	1	2	-	-	-	-	2	1	1	2	3
2	1	2	1	2	1	2	-	-	-	-	1	1	1	2	3
3	1	2	1	2	1	2	-	-	-	-	3	1	1	2	3
4	1	2	1	2	2	1	-	-	-	-	2	1	3	2	2
5	1	2	1	2	2	1	-	-	-	-	1	1	3	2	2
AVG	1.0	2.0	1.0	2.0	1.4	1.6	-	-	-	-	1.8	1.0	1.8	2.0	2.6

1-Low 2-Medium 3-High '-' – No Correlation

23PVP315	MEMS AND NEMS	L T P C 3 0 0 3

OBJECTIVES

- To study the concepts of micro electromechanical devices.
- To know the fabrication process of Microsystems.
- To understand the concept on the scope and recent development of the science and technology ofmicro- and nano-systems.
- To gain the physical knowledge underlying the operation principles and design of micro and nano- systems.
- To learn some typical or potentially applicable micro- and nano-systems at the frontier of the development of the field.

UNIT I OVERVIEW **9**

New trends in Engineering and Science: Micro and Nano scale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II MEMS FABRICATION TECHNOLOGIES **9**

Micro system fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT III MICRO SENSORS **9**

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV MICRO ACTUATORS **9**

Design of Actuators:Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate,Torsion bar,Comb drive actuators), Micromechanical Motors and pumps.Case study:Comb drive actuators.

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS **9**

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

OUTCOMES

Upon completion of the course, Students will be able to:

- Design micro and Nano scale systems.
- Discuss the MEMS fabrication technologies.
- Explain the Micro sensors.
- Analyze the operation of micro actuators and their applications.
- Design the atomic structures and quantum mechanics.

TEXT BOOKS

1. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2016.
2. Marc Madou, "Fundamentals of Microfabrication", CRC press2017.

REFERENCES

1. Stephen D. Senturia," Micro system Design", Kluwer Academic Publishers,2021.
2. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRCPress, 2017.

E-RESOURCES

1.https://nptel.ac.in/courses/117/105/117105082/(MEMS and Microsystems)

2.https://nptel.ac.in/courses/108/108/108108113/|(MEMS)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	2	1	-	-	-	-	-	-	2	1	3	2	3
2	1	1	2	1	-	-	-	-	-	-	1	1	3	2	3
3	1	1	2	1	-	-	-	-	-	-	3	2	3	2	3
4	1	1	2	1	2	-	-	-	-	-	2	2	3	2	3
5	1	2	2	1	2	-	-	-	-	-	1	2	3	2	3
AVG	1.0	1.2	2.0	1.0	2.0	-	-	-	-	-	1.8	1.6	3.0	2.0	3.0

1-Low 2-Medium 3-High '-' – No Correlation

23PGO201 **DISASTER MANAGEMENT** **L T P C**

3 0 0 3

OBJECTIVES

- To learn the basic conceptual understanding of disasters.
- To study different types of disasters.
- To learn about the disaster management techniques.
- To create awareness about disasters.
- To understand the concept of disaster risk assessment.

UNIT I: INTRODUCTION **9**

Definition and types of disaster Hazards and Disasters – Risk and Vulnerability in Disasters – Natural and Man-made disasters – Earthquakes, floods drought, landside, land subsidence, cyclones, volcanoes, tsunami, avalanches, global climate extremes – Man-made disasters: Terrorism, gas and radiations leaks, toxic waste disposal, oil spills, forest fires.

UNIT II: TYPES OF DISASTERS **9**

Study of important disasters Earthquakes and its types – Magnitude and intensity – Seismic zones of India – Major fault systems of India plate – Flood types and its management – Drought types and its management – Landside and its managements – Case studies of disasters in Sikkim (e.g) Earthquakes, Landside) – Social economics and environmental impact of disasters.

UNIT III: DISASTER MANAGEMENT **9**

Mitigation and Management techniques of Disaster – Basic principles of disasters management – Disaster Management cycle – Disaster management policy – National and State Bodies for Disaster Management – Early Warming Systems – Building design and construction in highly seismic zones – Retrofitting of buildings.

UNIT IV: DISASTER AWARENESS **9**

Training, awareness program and project on disaster management – Training and drills for disaster preparedness – Awareness generation program – Usages of GIS and Remote sensing techniques in disaster management.

UNIT V: RISK ASSESSMENT **9**

Mini project on disaster risk assessment and preparedness for disasters with reference to disasters in Sikkim and its surrounding areas.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Describe the basic conceptual understanding of disasters.
- Explain the different types of disasters.
- Analyze the disaster mitigation and management techniques.
- Discuss the importance of disaster awareness programs for disaster management.
- Analyze the risk behind the disasters.

TEXT BOOKS

1. Harsh K Gupta, Disaster Management, Universities Press Pvt. Limited, 9th edition, 2018.
2. Sulphey M.M., "Disaster Management", PHI Learning Private Limited, 4th Edition, 2017.
3. Damon P. Copola, "Introduction to International Disaster Management", Elsevier Inc, 1st Edition, 2016.

REFERENCES

1. Sharma S.C., "Disaster Management", Khanna Book Publishing Co. (P) Ltd., 5th Edition, 2018.
2. Gupta A.K., Nair S.S. and Chatterjee S. "Disaster Management and Risk Reduction: Role of Environmental Knowledge", Narosa Publishing House, 4th Edition, 2018.
3. Murthy D.B.N., "Disaster Management", Deep & Deep Publications, 3rd Edition, 2017.

E–RESOURCES

1. https://nptel.ac.in/courses/124/107/124107010/ (Disaster Management).
2. https://nptel.ac.in/courses/105/103/105103209/ (Plates and Shells)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	2	2	2	-	1	1	-	-	-	-	1	3	2	1
2	3	2	2	2	-	1	1	-	-	-	-	1	3	2	1
3	3	2	2	2	1	1	1	-	-	1	1	1	3	2	1
4	3	2	2	2	-	1	1	-	-	1	1	1	3	2	1
5	3	2	2	2	1	1	1	-	-	1	1	1	3	2	1
AVG	3.0	2.0	2.0	2.0	1.0	1.0	1.0	-	-	1.0	1.0	1.0	3.0	2.0	1.0

1-Low 2-Medium 3-High '-' – No Correlation

23PGO202 COST MANAGEMENT OF ENGINEERING PROJECTS L T P C

3 0 0 3

OBJECTIVES

- To understand the overview of cost management.
- To learn the different stages of project execution.
- To study the different analysis techniques adopted for project commissioning.
- To know the various pricing strategies followed in engineering projects.
- To study the different quantitative techniques used for cost management.

UNIT I: INTRODUCTION 9

Introduction and overview of the strategic cost management process – Cost concepts in decision making – Relevant cost, Differential cost, Incremental cost and Opportunity cost – Objectives of a Costing System – Inventory valuation – Creation of a database for operational control – Provision of data for decision making.

UNIT II: PROJECT 9

Meaning, different types, why to manage, cost overruns centres, various stages of project execution – Conception to commissioning – Project execution as conglomeration of technical and nontechnical activities – Detailed Engineering activities – Pre project execution main clearances and documents – Project team: Role of each member – Importance of project site – Data required with significance – Project contracts – Types and contents – Project execution – Project cost control – Bar charts and network diagram.

UNIT III: PROJECT COMMISSIONING 9

Mechanical and process – Cost Behavior and Profit Planning – Marginal Costing – Distinction between marginal costing and absorption costing – Break-even Analysis – Cost volume-Profit Analysis – Various decision-making problems – Standard Costing and Variance Analysis.

UNIT IV: PRICING STRATEGIES 9

Pareto Analysis – Target costing – Life cycle costing – Costing of service sector – Just-in-time approach – Material requirement planning – Enterprise resource planning – Total quality management and theory of constraints – Activity-based cost management – Bench marking – Balanced score card and value-chain analysis – Budgetary control – Flexible budgets – Performance budgets – Zero-based budgets – Measurement of divisional profitability pricing decisions including transfer pricing.

UNIT V: QUANTITATIVE TECHNIQUES FOR COST MANAGEMENT 9

Quantitative techniques for cost management - Linear programming - PERT/CPM - Transportation problems - Assignment problems - Simulation - Learning curve theory.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Explain the basics of cost management process.
- Analyze the detailed engineering activities associated in project execution.
- Apply suiltable analysis techniques for project commissioning.
- Discuss the various pricing strategies followed in project implementation.
- Analyze the different quantitative techniques used for cost management.

TEXT BOOKS

1. Charles T. Horngren, Srikant M. Datar and Madhav V. Rajan, "Cost Accounting A Managerial Emphasis", Pearson Education, 14th Edition, 2023.
2. Charles T. Horngren and George Foster, "Advanced Management Accounting", Pearson Education, 13th Edition, 2018.
3. Qiu Guo Lin, Cost management of engineering project, China Electric Power Press, 7th edition, 2017.

REFERENCES

1. Robert S Kaplan, Anthony A. Alkinson, "Management Accounting", Pearson Education, 4th Edition, 2022.
2. Ashish K. Bhattacharya, "Principles & Practices of Cost Accounting", PHI Learning Private Limited, 6th Edition, 2020.
3. Kenneth K Humpheys, Project and cost engineers' handbook (cost management), CRC Press, 4th edition, 2017.

E–RESOURCES

1. https://nptel.ac.in/courses/105/106/105106149/ (Types of Projects)
2. https://nptel.ac.in/courses/110/104/110104073/ (Cost Management for Projects)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	3	3	-	1	1	-	-	1	-	1	2	2	1
2	3	3	3	3	-	1	1	1	-	1	3	1	2	2	1
3	3	3	3	3	2	1	1	1	-	1	3	1	2	2	1
4	3	3	3	3	2	1	1	1	1	1	3	1	2	2	1
5	3	3	3	3	2	1	1	1	1	1	3	1	2	2	1
AVG	3.0	3.0	3.0	3.0	2.0	1.0	1.0	1.0	1.0	1.0	3.0	1.0	2.0	2.0	1.0

1-Low 2-Medium 3-High '-' - No Correlation

23PGO203 CONSTITUTION OF INDIA L T P C

3 0 0 3

OBJECTIVES

- To understand the basics of constitution law and constitutionalism.
- To learn the fundamental rights and duties.
- To know the constitution powers of union and state executives.
- To study the constitutional powers and procedures.
- To learn the powers and functions of public service commissions.

UNIT I: INTRODUCTION **9**

Meaning of the constitution law and constitutionalism – Historical perspective of the constitution of India – Preamble – Salient features and characteristics of the constitution of India – Citizenship.

UNIT II: FUNDAMENTAL RIGHTS **9**

Scheme of the fundamental rights – The scheme of the fundamental duties and its legal status – The directive principles of state policy – Its importance and implementation.

UNIT III: UNION AND STATE EXECUTIVE **9**

Federal structure and distribution of legislative and financial powers between the union and the states – Parliamentary form of Government in India – The constitution powers and status of the President of India – Governor – Appointment, powers and functions.

UNIT IV: CONSTITUTIONAL POWERS **9**

Amendment of the constitutional powers and procedure – The historical perspectives of the constitutional amendments in India – Emergency Provisions – National emergency – President Rule – Financial Emergency.

UNIT V: OTHER CONSTITUIONAL FUNCTIONARIES **9**

Election commission of India - Organization - Powers and functions - Union public service commission - State public service commission - Local self government.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Describe the features and characteristics of the constitution of India.
- Explain the importance of fundamental rights and duties.
- Analyze the constitution power of union and state executives.
- Discuss the amendment of constitutional powers and procedure.
- Examine the powers and functions of union and state public service commission.

TEXT BOOKS

1. Durga Das Basu, "Introduction to the Constitution of India", Lexis Nexis Publishers, 24th Edition, 2019.
2. Subhash C. Kashyap," Our Constitution", National Book Trust, 5th Edition, 2021.
3. P M Bakshi, The constitution of India, Universal Law Publishing, 14th edition, 2017.

REFERENCES

1. M.Laxmikanth, "Indian Polity", McGraw Hill Publications, 7th Edition, 2023.
2. Granville Austin, "The Indian Constitution: Cornerstone of a Nation", OUP India, 8th Edition, 2017.
3. V N Shukla, Constitution of India, Eastern Book Company, 4th Edition, 2019.

E–RESOURCES

1. https://nptel.ac.in/courses/129/106/129106002/(Constitution of India)
2. https://nptel.ac.in/courses/129/106/129106003/(Constitutional Studies)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	2	2	1	-	1	-	1	1	1	-	1	2	1	1
2	3	2	2	1	-	1	-	1	1	1	-	1	2	1	1
3	3	2	2	1	-	1	-	1	1	1	-	1	2	1	1
4	3	2	2	1	-	1	-	1	1	1	-	1	2	1	1
5	3	2	2	1	-	1	-	1	1	1	-	1	2	1	1
AVG	3.0	2.0	2.0	1.0	-	1.0	-	1.0	1.0	1.0	-	1.0	2.0	1.0	1.0

1-Low 2-Medium 3-High '-' - No Correlation

23PGO204 **BUSINESS ANALYTICS** **L T P C**

3 0 0 3

OBJECTIVES

- To learn the overview of business analysis.
- To know the importance of project life cycle and product life cycles.
- To understand the different types of requirements in business analytics.
- To study the various analysis techniques for transforming requirements.
- To learn about finalizing requirements.

UNIT I: BUSINESS ANALYSIS **9**

Overview of business analysis – Overview of requirements – Role of the business analyst – Stakeholders: the project team, management, and the front line – Handling stakeholder conflicts.

UNIT II: LIFE CYCLES **9**

Systems development life cycles – Project life cycles – Product life cycles – Requirement life cycles.

UNIT III: FORMING REQUIREMENTS **9**

Overview of requirements – Attributes of good requirements – Types of requirements – Requirement sources – Gathering requirements from stakeholders – Common requirements documents.

UNIT IV: TRANSFORMING REQUIREMENTS **9**

Stakeholder Needs Analysis – Decomposition Analysis – Additive/Subtractive Analysis – Gap Analysis – Notations (UML & BPMN) – Flowcharts – Swim Lane Flowcharts – Entity-Relationship Diagrams – State-Transition Diagrams – Data Flow Diagrams – Use Case Modeling – Business Process Modeling.

UNIT V: FINALIZING REQUIREMENTS **9**

Presenting requirements - Socializing requirements and gaining acceptance - Prioritizing requirements - Managing requirements Assets - Change control - Requirement tools - Recent trends in embedded and collaborative business intelligence - Visual data recovery - Data storytelling and data journalism.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Explain the role of business analyst in business proposals.
- Examine the necessity of product life cycle and requirement life cycle.
- Describe the overview of forming requirements.
- Analyze various transforming requirements used in business analytics.
- Apply requirement tools for finalizing requirements.

TEXT BOOKS

1. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, "Business analytics Principles, Concepts, and Applications", Pearson FT Press, 3rd Edition, 2019.
2. James R Evans, "Business Analytics", Pearson FT Press, 3rd Edition, 2020.
3. Wayne L. Winston, "Business Analytics: Data analysis & decision making", South Western College Publishing, 6th Edition, 2017.

REFERENCES

1. Swain Scheps , "Business Intelligence for Dummies", Dummies Publishers, 4th Edition, 2018.
2. Ger Koole, "An Introduction to Business Analytics", MG Books, 1st Edition, 2019.
3. Walter R. Paczkowski, "Business Analytics: Data Science for Business Problems", Springer International Publishing, 1st Edition, 2022.

E–RESOURCES

1. https://nptel.ac.in/courses/110/107/110107092/ (Business analytics and data mining modeling)
2. https://nptel.ac.in/courses/110/105/110105089/ (Business analytics for management decision)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	3	3	2	1	-	-	-	1	2	1	3	2	1
2	3	3	3	3	2	1	-	1	1	1	2	1	3	2	1
3	3	3	3	3	2	1	-	1	1	1	2	1	3	2	1
4	3	3	3	3	2	1	-	1	1	1	2	1	3	2	1
5	3	3	3	3	2	1	-	1	1	1	2	1	3	2	1
AVG	3.0	3.0	3.0	3.0	2.0	1.0	-	1.0	1.0	1.0	2.0	1.0	3.0	2.0	1.0

1-Low 2-Medium 3-High '-' - No Correlation

23PGO205 DIGITAL MARKETING L T P C

3 0 0 3

OBJECTIVES

- To understand the origin of digital marketing.
- To learn the different types of social media marketing.
- To know the techniques adopted for search engine optimization.
- To study the importance of facebook marketing and mobile marketing in business.
- To learn the tools and methods of web analytics.

UNIT I: INTRODUCTION & ORIGIN OF DIGITAL MARKETING **9**

Traditional v/s digital marketing – Digital marketing strategy – The P-O-E-M framework – Segmenting & customizing messages – The digital landscape – Digital advertising market in India – Skills required in digital marketing – Digital marketing plan.

UNIT II: SOCIAL MEDIA MARKETING **9**

Meaning, purpose, types of social media websites – Blogging: types of blogs – Blogging platforms & recommendations – Social media engagement – Target audience – Sharing content on social media – Do's and don'ts of social media.

UNIT III: SEARCH ENGINE OPTIMIZATION **9**

Meaning – Common SEO techniques – Understanding search engines – Basics of keyword search – Google rankings – Link building – Steps to optimize website – Basics of Email marketing: Types of Emails – Mailing list – Email marketing tools – Email deliverability & Email marketing automation.

UNIT IV: FACEBOOK MARKETING **9**

Introduction – Facebook for business – Anatomy of an Ad campaign – Role of adverts – Types & targeting – Adverts budget & scheduling – Adverts objective & delivery – LinkedIn marketing- introduction & importance – LinkedIn strategies – Sales leads generation using LinkedIn – Content strategies – Mobile marketing – Introduction – Mobile usage – Mobile advertising – Mobile marketing tool kit – Mobile marketing features.

UNIT V: UNDERSTANDING WEB ANALYTICS **9**

Purpose, history, goals & objectives - Web analytic tools & methods - Web analytics mistakes and pitfalls - Basics of content marketing: Introduction - Content marketing statistics - Types of content - Types of blog posts - Content creation - Content optimization - Content management & distribution - Content marketing strategy - Content creation tools and apps - Challenges of content marketing.

TOTAL: 45 PERIODS

OUTCOMES

Upon completion of the course, Students will be able to:

- Explain the strategy of digital marketing.
- Describe the purpose of social media marketing.
- Apply the suitable technique for search engine optimization.
- Examine the importance of facebook marketing and linkedin marketing in business.
- Analyze the mistakes and pitfalls of web analytics.

TEXT BOOKS

1. Rajendra Nargundkar and Romi Sainy "Digital Marketing: Cases from India", Notion Press, 1st Edition, 2018.
2. Damian Ryan, "Understanding Digital Marketing: Marketing Strategies for Engaging the Digital Generation", Kogen Page Publishers, 3rd Edition, 2018.
3. Simon Kingsnorth, "Digital Marketing Strategy: An integrated approach to online marketing", Kogen Page Publishers, 2nd Edition, 2017.

REFERENCES

1. Hermawan Kartajaya, Philip Kotler and Iwan Setiawan , "Marketing 4.0 : Moving from Traditional to Digital", Wiley Publishers, 1st Edition, 2018.
2. Seema Gupta, "Digital Marketing", McGraw Hill Publications, 3rd Edition, 2022.
3. Prabir Rai Chaudhuri, "What is digital marketing: A comprehensive guide", WMG Publishing, 1st Edition, 2022.

E–RESOURCES

1. https://onlinecourses.swayam2.ac.in/cec19_mg23/preview (Basics of Digital Marketing)
2. https://onlinecourses.swayam2.ac.in/ugc19_hs26/preview (Digital Marketing)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	3	3	3	2	1	-	1	1	1	1	1	3	2	1
2	3	3	3	3	2	1	-	1	1	1	1	1	3	2	1
3	3	3	3	3	2	1	-	1	1	1	1	1	3	2	1
4	3	3	3	3	2	1	-	1	1	1	1	1	3	2	1
5	3	3	3	3	2	1	-	1	1	1	1	1	3	2	1
AVG	3.0	3.0	3.0	3.0	2.0	1.0	-	1.0	1.0	1.0	1.0	1.0	3.0	2.0	1.0

1-Low 2-Medium 3-High '-' - No Correlation

23PGO206 ELECTRONICS FOR SOLAR POWER L T P C
3 0 0 3

OBJECTIVES

- To study the behavior of photovoltaic solar energy systems, focusing on the behavior of "stand-alone" systems.
- To learn a first order, conceptual design of a stand-alone system for a location anywhere in India
- To know the hardware elements and their behavior.
- To acquire the knowledge of battery for a PV system and battery sizing
- To understand the standalone and grid tied PV system

UNIT I INTRODUCTION TO SOLAR POWER 9

Semiconductor – properties - energy levels - basic equations of semiconductor devices physics - Basic characteristics of sunlight - Solar angles - day length - angle of incidence on tilted surface – Sun path diagrams – Equivalent circuit of PV cell, PV cell characteristics (VI curve, PV curve) - Maximum power point, Vmp, IMP, Voc, ISC – types of PV cell - Block diagram of solar photo voltaic system, PV array sizing.

UNIT II DC-DC CONVERTER 9

Principles of step-down and step-up converters – Analysis and design issues of buck, boost, buckboost and Cuk converters – time ratio and current limit control – Full bridge converter – Resonant and quasi – resonant converters.

UNIT III MAXIMUM POWER POINT TRACKING 9

Direct Energy transmission, Impedance Matching, Maximum Power Point Tracking (MPPT) - Function of MPPT, P&O method, INC Method, Fractional Open circuit voltage method, Fractional short circuit current method, parasitic capacitance and other MPPT techniques, Development of hardware, algorithms using processors for Standalone and Grid tied systems.

UNIT IV BATTERY 9

Types of Battery, Battery Capacity – Units of Battery Capacity-impact of charging and discharging rate on battery capacity-Columbic efficiency-Voltage Efficiency, Charging – Charge Efficiency, Charging methods, State of Charge, Charging Rates, Discharging - Depth of discharge-Discharge Methods, Circuits for Battery Management System (BMS), selection of Battery and sizing.

UNIT V SIMULATION OF PV MODULE & CONVERTERS 9

Simulation of PV module - VI Plot, PV Plot, finding VMP, IMP, Voc, Isc of PV module, Simulation of DC to DC converter -buck, boost, buck-boost and Cuk converters, standalone and grid tied photo voltaic system.

TOTAL:45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, Students will be able to:

- Explain the solar power characteristics at a given location
- Analyze the design and realize dc-dc converters for solar power utilization
- Explain the algorithms for improving solar power utilization
- Discuss the battery issues and selection
- Examine the design and simulate PV systems to validate its performance.

TEXT BOOKS

1. Chetan Singh Solanki, "Solar photovoltaic: fundamentals technologies and applications", PHI Ltd., 2019.
2. Tommarkvart, Luis castaner, "Solar cells materials, manufacture and Technologies and operation", Elseiver,2015.

REFERENCES:

1. G.D.Rai," Solar energy utilization",Khanna publishes,2019.
2. Ned Mohan, Undeland and Robbin , " Power Electronics: converters, application and design", John Wiley and sons.Inc, Network,2015.

E-RESOURCES

1. https://archive.nptel.ac.in/courses/117/108/117108141/ (Design of photovoltaic system)
2. https://onlinecourses.nptel.ac.in/noc20_ph21/preview (Solar Photovoltaic Fundamentals, Technology And Applications)

Mapping of Cos-Pos & PSOs

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	1	1	1	1	1	-	-	-	-	-	2	1	3	2	3
2	1	1	1	1	2	-	-	-	-	-	2	1	3	2	3
3	1	1	1	1	2	-	-	-	-	-	3	2	3	2	3
4	1	1	2	1	2	-	-	-	-	-	2	2	3	2	3
5	1	2	2	1	2	-	-	-	-	-	1	1	3	2	3
AVG	1.0	1.2	1.6	1.0	1.8	-	-	-	-	-	2.0	1.4	3.0	2.0	3.0

1-Low 2-Medium 3-High '-' – No Correlation

CURRICULUM AND SYLLABI

FOR M.E. DEGREE PROGRAMMES

(For the Students Admitted in the Academic Year 2023 – 2024 onwards)

CREDIT SUMMARY

M.E. – VLSI DESIGN

Category	Credits Per Semester				Credit Total
	I	II	III	IV	
FC	7	-	-	-	7
PC	11	10	-	-	21
PE	3	6	11	-	20
OE	-	3	-	-	03
EEC	0	1	6	12	19
Total	21	20	17	12	70